ADA-R9100 User Manual

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1 Product Description

The ADA-R9100 is a 1U 19" Rack Mount appliance based around the AMD Ultrascale+ VU2P Ultra Low Latency FPGA.

This appliance is designed to provide the lowest latency access to the highest number of ultra-low latency GTF transceivers that are the unique feature of the VU2P device. 32 extremely low latency channels are provided via SFP+ connections on the front panel, with trace delays as low as 464ps. Another 40 low latency channels are provided via QSFP28 connections on the front panel, with trace delays as low as 1.456ns.

Multiple clock jitter attenuators are available on appliance FPGA board to allow source synchronous clocking of GTF receivers. The FPGA board also features 16GB DDR4 SODIMM and 576Mb of QDRII+ SRAM.

The appliance is data center deployment ready and can be remotely managed using the embedded ASRockRack ROME4ID-2T motherboard. This platform features an ATSPEED BMC that allows remote management and power cycling of the system. The CPU sub-system features an AMD EPYC7002 series processor, 32GB DDR4 and 250GB NVMe pre-installed with Ubuntu Linux OS. This system is powerful enough to run the AMD Vivado toolset for advanced remote debug and development.

Additional comprehensive system monitoring of the complete appliance is available on standby and fully powered up via Ethernet, IPMI and USB functionality. The CPU sub-system can connect to the FPGA via PCIe Gen3x8.

The appliance features a dual redundant power supply, for server-class reliability.

Figure 1 : ADA-R9100 Appliance

Description	Measure
Total Dy	540 mm
Total Dx	484 mm
Total Dz	44 mm
Weight	11.28 kg
PSU Rating	500W

Table 1 : Mechanical Dimensions (Without Rails)

2 HW Modules

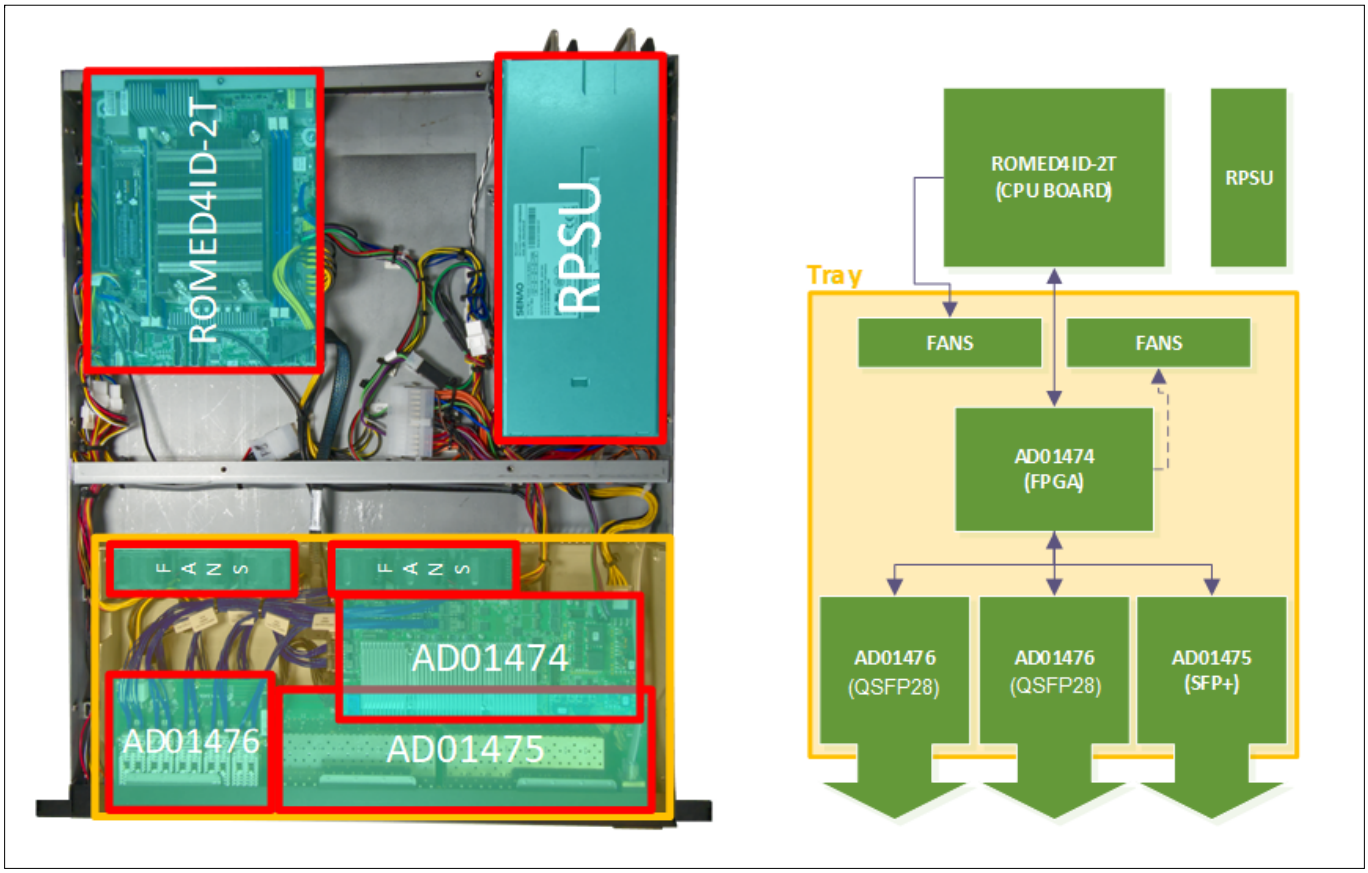

Figure 2 : R9100 HW modules

2.1 FPGA and SFP/QSFP

The ADM-R9100 AD01474 configurable network switch accelerator is composed of 3 Alpha-Data-designed circuit boards. The FPGA board (AD01474) attaches directly to an SFP breakout board (AD01475) and is cabled to two QSFP boards (AD01476).

The AD01474 is fitted with an AMD Virtex UltraScale+ VU2P, an ultra-low latency FPGA device.

The low-latency lanes are driven by the Xilinx GTF transceivers. The ADA-R9100 has been tested at both 10.3125Gbps and 25.78125Gbps for each low latency lane.

The SFP/QSFP connections at the front are rated at Power Level II (1.5W max) for SFP+ ports, and Power Level 7 (5W max) for QSFP28 ports.

The system is modular, and the AD01474/75/76 subsystem is fitted on a detachable tray for serviceability.

2.2 CPU board

Featuring AMD's ROMED4ID-2T server grade mini-ITX motherboard, the R9100 supports all the typical services like Web, KVM, SSH, LDAP, RADIUS services, through its BMC processing subsystem.

Remote access with video support is through the KVM server, and it can be remotely launched from the available web server when the BMC is on (on standby too).

For more information, refer to ROMED4ID-2T's user manual:
https://www.asrockrack.com/general/productdetail.asp?Model=ROMED4ID-2T#Manual

2.3 Redundant PSU (RPSU)

The system is fitted with a 500W 1+1 redundant power supply (ATX compliant), compatible with CPU boards with 24P connectors. The RSPU is PMBus/SMBUS 1.2 compliant.

To operate the RPSU remotely (query state, switch ON/OFF, etc..), see Section 11.

For input specification see Section 3, items 15 and 16.

For additional information and technical details on the RSPU, contact support@alpha-data.com.

3 HW Interfaces

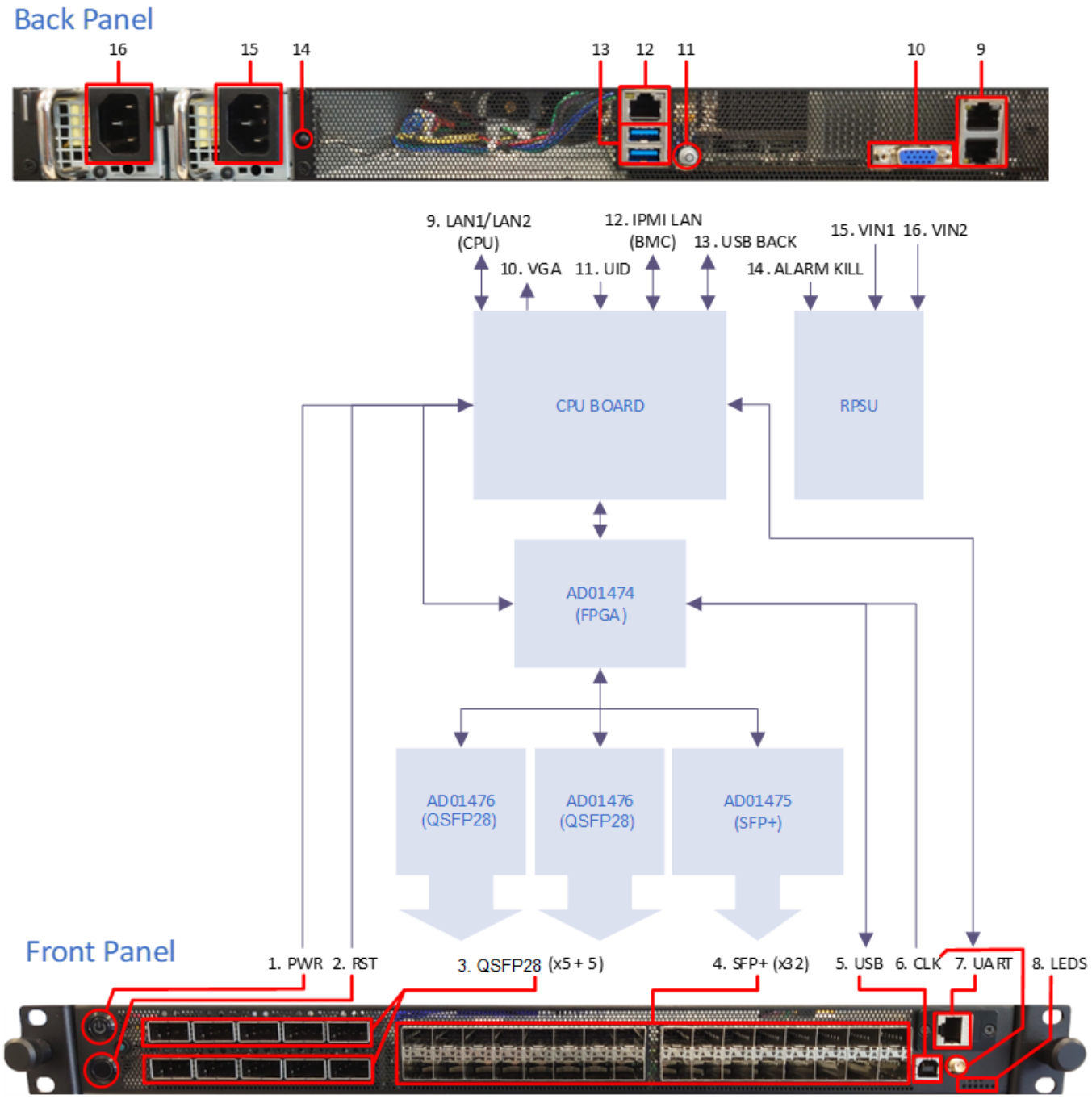

Figure 3 : Interfaces

Front Panel

1 PWR: Power ON/OFF button/indicator. This is a momentary action pushbutton with LED indication. The two independent processing systems (ROMED4ID-2T and AD01474) remain on standby until the button is pressed. The indicator lights up when the system is powered on.

Note:
This is an ACPI-compliant operating system, when the power button is used to shut the system down, the operating system performs a graceful shut down and the system power is turned off. If the button is pushed and held for 3-5s, an immediate shutdown is performed.

2 RST: ROMED4ID-2T's reset. This is a momentary action pushbutton. It performs a system reset when pressed.

3 QSFP28: Ethernet/Optical connections. There are 5 cages per row and 4 lanes per cage (x40 channels). Up to a 25Gbps bandwidth per channel. Cages are rated at Power Level 7 (**5W max**). Each cage has its own LED section. See Section 7.5.3 for the meaning of these LEDs.

4 SFP+: Ultra-low latency for Ethernet/Optical connections (x32 channels). Up to a 25Gbps bandwidth per channel. Cages are rated at Power Level II (**1.5W max**). Each cage has its own LED section. See Section 7.5.2 for the meaning of these LEDs.

5 USB: USB 2.0 connection for FPGA programming and debug. Accepts standard USB-B connection. See section Section 7.2 for using the interface.

6 CLK: 1PPS input clock reference for synchronization with external equipment. Accepts standard SMA connector (male).

7 UART: Serial port for management access to the appliance. Accepts a null-modem cable***** (also known as rollover cable). See section Section 7.3 for more information on using this interface.

Note:
***WARNING! DO NOT** connect a standard network cable to this RJ45 interface! this is an out-of-band connection and connecting it to a network device may damage its internal circuits.

8 LEDs: System LEDs. A total of 9 LED lights are provided signalling system state and user information. See Section 7.5.1 for the meaning of these LEDs.

Back Panel

9 LAN1/LAN2 (CPU): Ethernet port for the CPU board. These are ROMED4ID-2T's 10GbE network interfaces.

10 VGA: VGA port. D-Sub cable connection.

11 UID: Unit Identification purpose LED/Switch. Press to locate the server in a rack of servers.

12 IPMI LAN (BMC): Ethernet port for the BMC processor. This is ROMED4ID-2T's management network interface for remote system monitoring and control.

13 USB (back): USB 3.2 Gen1 Port.

14 ALARM KILL: Alarm kill switch. It shuts down the RSPSU alarm (it goes off when a fault is detected in a power module).

15 VIN1: AC inlet for 500W 1+1 redundant power supply's module 1. Input Voltage and Frequency: to be connected to a 115Vac or a 230Vac (50/60Hz) lines***** with a cable rated at 15A/250VAC.

16 VIN2: AC inlet for 500W 1+1 redundant power supply's module 2. Input Voltage and Frequency: to be connected to a 115Vac or a 230Vac (50/60Hz) lines***** with a cable rated at 15A/250VAC.

Note:
*****Maximum and minimum input voltage and frequency ratings for the RSPU (sinusoidal): 100~240 VAC full range, with ±10% tolerance. Input frequency ranges from 47Hz~63Hz

4 Installing the Chassis

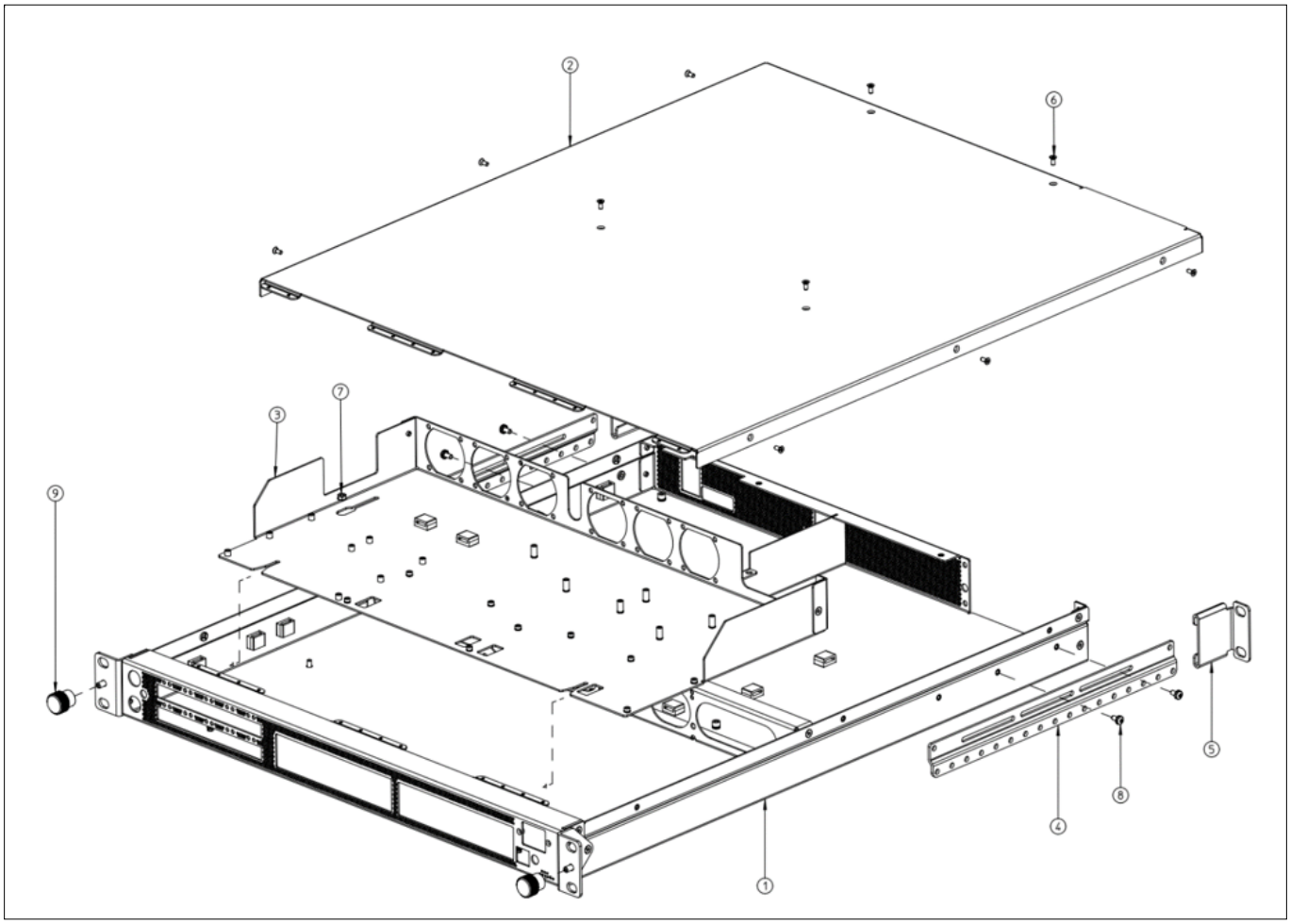

Figure 4 : Chassis Elements

Item	Description	Qty
1	Chassis Base	1
2	Top Cover	1
3	Mounting Tray	1
4	Rack Adjustable Rail	2
5	Rack Adjustable Hook Bracket	2
6	M2.5x6 CSK POSI Black	10
7	M3 KEPS Hex Nut	2
8	M3x6 PAN Head Posi	4
9	Thumb Nut (WDS8151-213)	2

Table 2 : Mounting Components

Start by attaching the rear mount support brackets: the two right angle mount brackets (5) need to be attached to the rear side of the rack first. Use the provided hardware. Check for the correct aligment in the 1U slot:

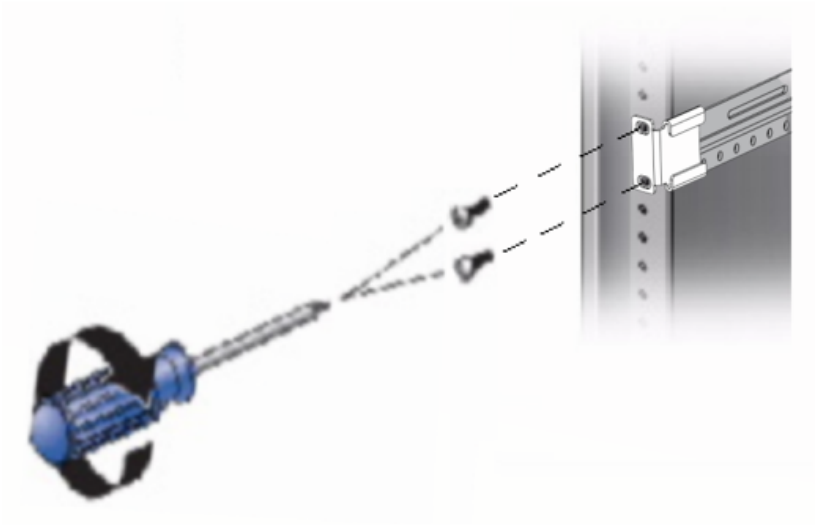

Figure 5 : Securing the mount support to the rack

Now, fit the mounting rail (4), but not too tight (allow some horizontal movement) and slide it all the way back for maximum extension, then slide the unit in the rack until solidly supported by the previously installed rear brackets (5). Check the slack and adjust the rails for a good fitting of the front panel (as depicted below):

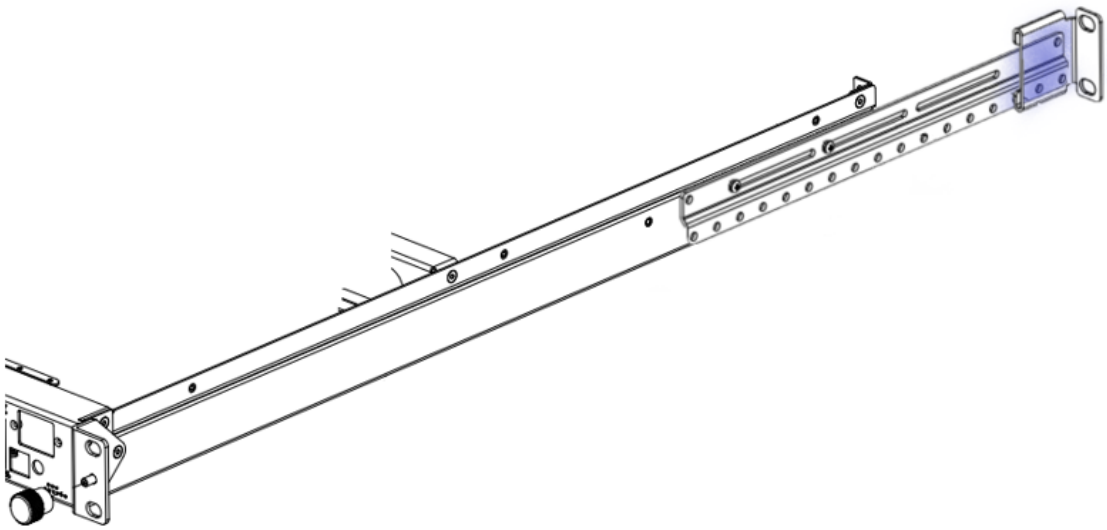

Figure 6 : Adjusting the rails extension to the rack depth

Screw up the front panel for a tight fit. Finally, secure the rails by tightening up the screws that were not fully tightened in step 3. That is the unit secured in the rack.

Note:
Always try to install the heaviest equipment near the bottom of the rack to prevent the rack from tipping over when the chassis is pulled out on its rails.

Note:
When possible, install anti-tip legs to the rack to also prevent tipping, or some other anti-tip device which protects the enclosure from tipping when servers and shelves are extended.

5 Operating System and Pre-installed SW

The R9100 comes with **Ubuntu 18.04.6 LTS** preinstalled. It is configured with a graphical desktop and will automatically boot into it when operated locally. SSH is enabled for remote access too.

The default user account details are provided in the delivery sheet for this product. Contact support@alpha-data.com for additional information and requests.

Additional preinstalled SW list:

- Vivado Lab 2022.2
- avr2util-s (avr2util-s-4.19.0)
- ADXDMA driver module (adxdma-driver-linux-0.11.0_ad01474)
- Minicom

6 Powering the System Up

The R9100 is equipped with a 1+1 redundant power supply unit (RSPU), and as such both redundant modules need to be sourced for a reliable 24/7 server operation. For best performance, plug both modules into the power lines before turning the system on (see Section 3, items 15 and 16).

> **Note:**
> The RSPU **does not** have a power button, as this is handled by the ON/OFF button of the R9100 (ACPI system)

The LED by the power socket on the RPSU will flash green if the operation of the corresponding module is normal as soon as the RPSU is sourced (i.e.: plugged into the power lines), and it will turn red if a fault occurs.

The system ON/OFF switch is handled by a momentary pushbutton up front (see Section 3, item 1)

If the system is turned ON with one of the redundant modules disconnected (or faulty), an acoustic alarm will go off. This means that the system has detected the condition of a missing module, and while it can normally continue its operation with a single module, it is strongly recommended to plug the other module in (or hot-swap it when it is faulty).

> **Note:**
> To disregard the alarm and shut it off, press the button in the middle of the RPSU once (see Section 3, item 14)

Contact support@alpha-data.com for extended information on the RPSU

6.1 Standby operation

The system will go into standby mode right after the RPSU has been sourced(i.e., plugged into the power lines). The system is ready to be operated by then. See a summary of the active subsystems and interfaces below:

Subsystem	Active in rail/s(V)	User Access	Active I/F
BMC	5Vsb	Enabled	IPMI(BMCEth)/ RDP(BMCEth)/ UART(F)
CPU	5Vsb	Disabled	-
System monitor (FPGA)	5Vsb	Enabled	USB(F)/ USB(B)*/ IPMI(PCIe)
SFP	-	Monitor	USB(F)/ IPMI(Mod_Abs)
QSPF	-	Monitor	USB(F)/ IPMI(ModPrsL)
RPSU	N/A	Enabled	IPMI(PMBus)

Table 3 : System Status at Standby Power

> **Note:**
> If USB(F) - front panel USB connection - is connected (see Section 3, item 5), then USB(B) (or internal USB connection between the CPU System and the AD01474) will be lost momentarily until USB(F) is disconnected. System Monitor queries in this case will need to be run through IPMI.

6.2 Full-power operation

The system will enter the full-power mode only after the power ON/OFF button of the R9100 has been pressed while in standby mode (see Section 3, item 1). The system will boot into the preinstalled Ubuntu OS and show the login screen with the default user. All subsystems are enabled and accessible in this mode. See a summary of the active subsystems and interfaces below:

Subsystem	Active in rail/s (V)	User Access	Active I/F
BMC	5Vsb	Enabled	IPMI(BMCEth)/ RDP(BMCEth)/ UART(F)
CPU	3.3/5Vsb/12	Enabled	IPMI(BMCEth)/ CPUEth(Full)/ UART(F)
System monitor (FPGA)	5Vsb/12	Enabled	USB(F)/ USB(B)*/ IPMI(PCIe)
SFP	3.3	Enabled	USB(F)/ IPMI(Full)
QSPF	3.3	Enabled	USB(F)/ IPMI(Full)
RPSU	N/A	Enabled	IPMI(PMBus)

Table 4 : System Status at Full-Power

For a complete list of user profiles and power domains for system monitoring, see the System Sensors and Monitoring appendix.

7 Feature Description

7.1 IPMI PCIe/I2C

There is an internal IPMI (PCIe/I2C) connection between the CPU System and the AD01474. It can handle the IPMI commands locally from the CPU system as a local I2C device, or remotely through the IPMI tree by the BMC/CPU Ethernet connections.

7.2 USB front/back

There is a common USB connection to the AD01474 that is split in two in the system: an internal USB connection with no external port (between the CPU System and the AD01474), and a direct one with a USB B port in the front panel of the R9100. The latter provides direct access for a quick local operation without needing to log into the system (i.e.: operator with a laptop). For operating the one on the CPU side, login into Ubuntu is required.

The AD01474 utilizes the Digilent USB-JTAG converter which is supported by the AMD software tool suite. The two cases based on the connection are:

- Direct (external): Simply connect a USB B type cable between the front panel USB port (see Section 3, item 5) and a host computer with Vivado installed. Vivado Hardware Manager will automatically recognize the FPGA and allow you to configure it, and the SPI configuration Flash memory.
- Ubuntu (internal): Vivado Lab automatically detects USB connection to the AD01474 (see Section 9).

Both USB connections handle system monitor queries the FPGA programming/debugging. For system monitor usage, see Section 8.

> **Note:**
> If USB(F) - front panel USB connection - is connected (see Section 3, item 5), then USB(B) (or internal USB connection between the CPU System and the AD01474) will be lost momentarily until USB(F) is disconnected. System Monitor queries in this case will need to be run through IPMI.

7.3 Management serial port (UART)

This is an RS2320-compliant serial port on an RJ45 connection (Section 3, item 7). This allows a connection with a PC running a terminal emulation SW by means of a null-modem cable (also known as **rollover cable**, where all the pins on one end (1-8) appear inverted with respect to the opposite end (8-1)). Same as the console port of LAN Cisco switches/routers.

> **Note:**
> ***WARNING! DO NOT** connect an standard network cable to this RJ45 interface! this is an out-of-band connection and connecting it to a network device may damage its internal circuits.

Typically, you can send/receive files and run system commands with a terminal emulation SW like Minicom. This SW comes pre-installed with Ubuntu on the R9100.

To run Minicom on the R9100 and listen to incoming connections, execute the following commands:

```
sudo chmod 666 /dev/ttyS0
minicom -b 115200 -D /dev/ttyS0
```

> **Note:**
> Ubuntu will map the serial port to **/dev/ttyS0** by default. The connection speed is **115200** bauds on the R9100.

Note:
You will need to **deactivate flow control** in Minicom by:
Ctr-A Z --> Configure Minicom(O) --> Serial port setup --> HW flow control --> **OFF**
--> SW flow control --> **OFF**
Alternatively, run minicom -s to change parameters or modify the file **minirc.dlf** with the following lines to make changes persistent:
pu port /dev/ttyS0
pu rtscts No

7.4 Input clock reference

Input SMA port for a 1PPS synchronization signal (Section 3, item 6). This can be used to synchronize with external devices and instrumentation.

This clock is connected to the FPGA at pin H32, net name 1PPS_1V8 as shown in Complete AD01474 pinout.

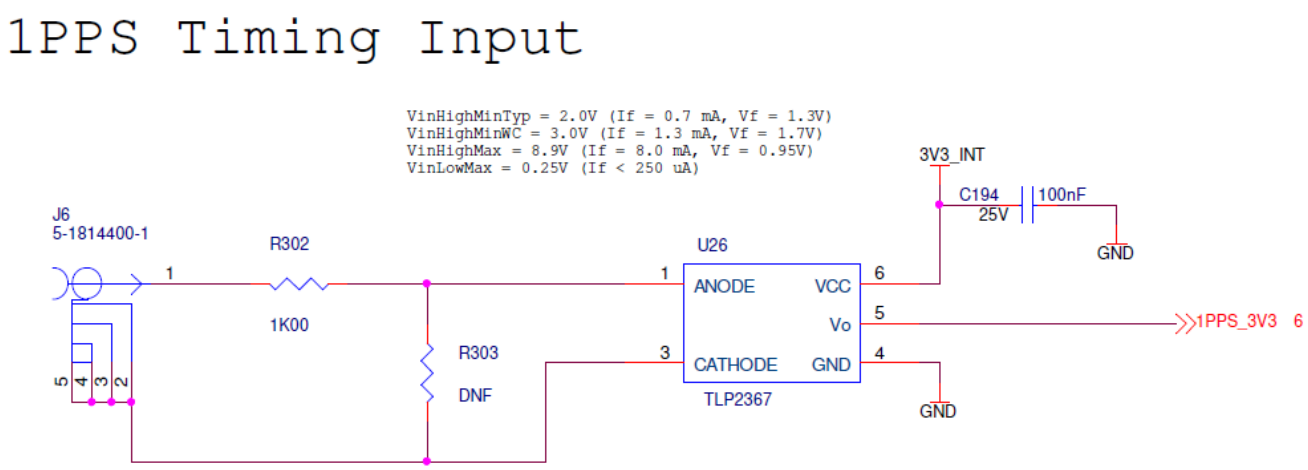

Figure 7 : 1PPS circuit

7.5 LEDs

7.5.1 System LEDs

There are 9 system LEDs on the ADA-R9100, 6 of which are general purpose and whose meaning can be defined by the user. The other 3 have fixed functions described below:

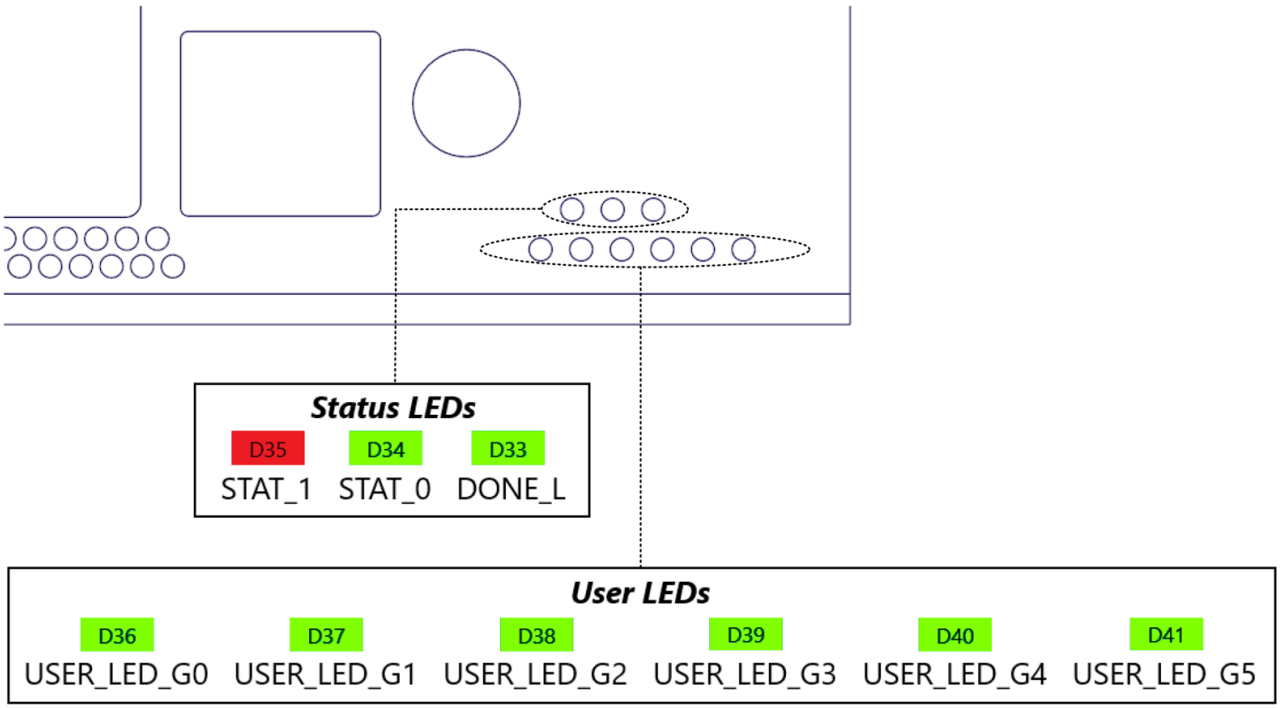

Figure 8 : Front Panel LEDs

Comp. Ref.	Function/Net Name	ON State	OFF State
D36	USER_LED_G0_1V8	User defined '0'	User defined '1'
D37	USER_LED_G1_1V8	User defined '0'	User defined '1'
D38	USER_LED_G2_1V8	User defined '0'	User defined '1'
D39	USER_LED_G3_1V8	User defined '0'	User defined '1'
D40	USER_LED_G4_1V8	User defined '0'	User defined '1'
D41	USER_LED_G5_1V8	User defined '0'	User defined '1'
D33	DONE_L	PL is configured	PL is not configured
D34	Status 0	See Status LED Definitions	
D35	Status 1	See Status LED Definitions	

Table 5 : LED Details

7.5.2 SFP+ cages LEDs

There are 2 LEDs per SFP+ cage, arranged in pairs of 2 together (for the top and bottom cages). The two on the right-hand side are the "module present" signal of each cage, whereas the two on the left are the "link up"(or user definable) of either one. Find the arrangement below:

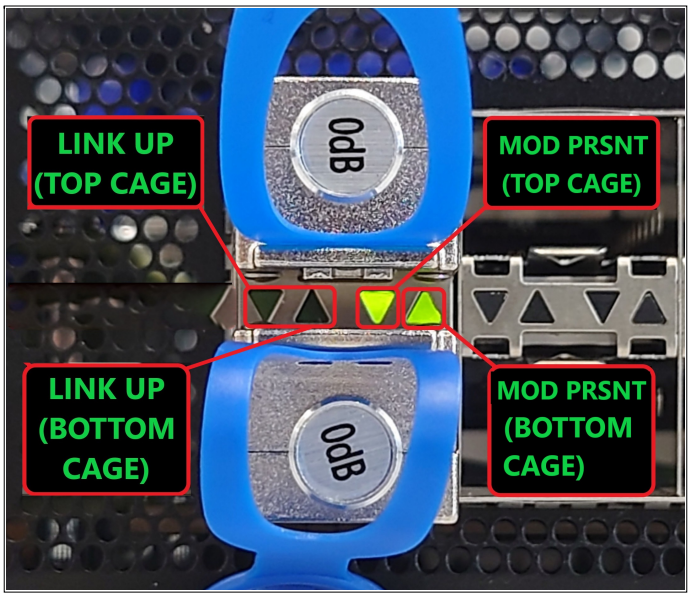

Figure 9 : SFP LEDs

7.5.3 QSFP28 cages LEDs

There are 2 LEDs per QSFP28 cage. These are located at the top of each cage. The one on the right-hand side is the "link up" (or user-definable) signal, and the one on the left is the "module present" signal of that cage. Find the arrangement below:

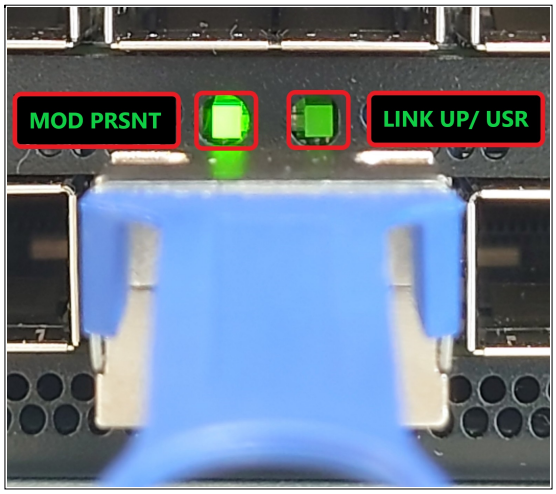

Figure 10 : QSFP LEDs

7.6 QSFP/SFP

See section IPMI PCIe/I2C for details on sideband I2C communication with the QSFP/SFP cages and control of the "link up" LEDs on the front panel.

Trace lengths for the SFP links and the associated estimated propagation delay for each lane are listed in appendix SFP delays. These delays were calculated using the estimated propagation delay of Megtron 6 PCB laminate, which is 5.85ps/mm.

Trace lengths for the QSFP links and the associated estimated propagation delay for each lane are listed in appendix QSFP delays. These delays were calculated using the estimated propagation delay of Megtron 6 PCB laminate combined with the propagation delay of the Samtec twinax cable, which are 5.85ps/mm and 4.79ps/mm respectively.

See below the arrangement of the QSFP/SFP cages and their connections to the FPGA transceivers (QUADS) in the AD01474.

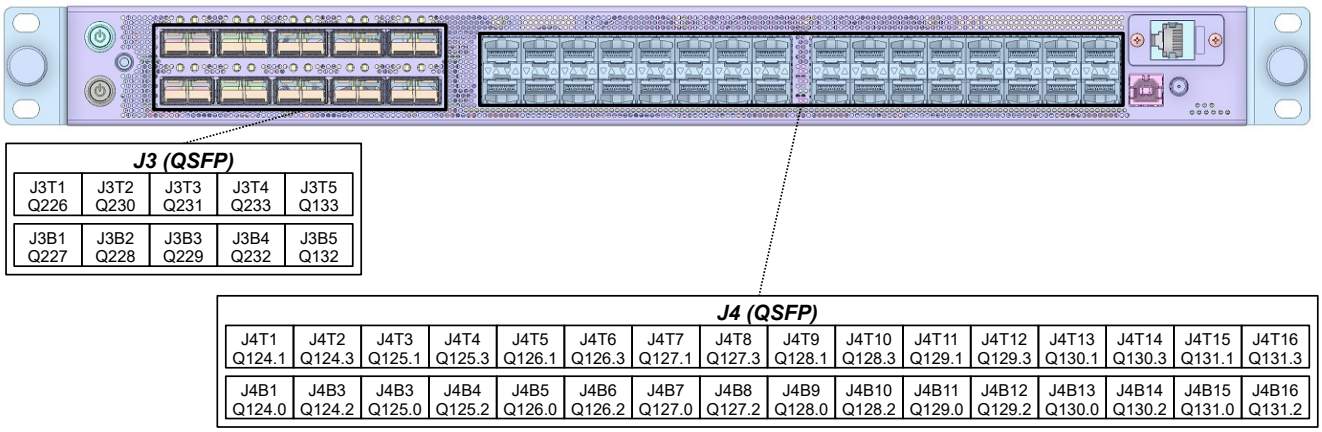

Figure 11 : Front Panel QSFP/SFP connections to the AD01474

7.7 Clocking

The ADM-R9100 provides flexible reference clock solutions for the many multi-gigabit transceiver quads, DDR4, QDRII+ banks, and PL fabric.

The reprogrammable clocks from the LMK61E2 are reconfigurable from the USB front/back interface by using Alpha Data's avr2util utility. This allows the user to configure almost any arbitrary clock frequency during application run time for the SFP/QSFP reference clock. The maximum clock frequency for the LMK61E2 is 900MHz.

There are four Si5324 jitter attenuators. These can provide clean and synchronous clocks to all of the QSFP and SFP quad locations at many clock frequencies. The Si5324 can be reconfigured over I2C using a controller embedded in the FPGA design.

All clock names in the section below can be found in Complete AD01474 pinout.

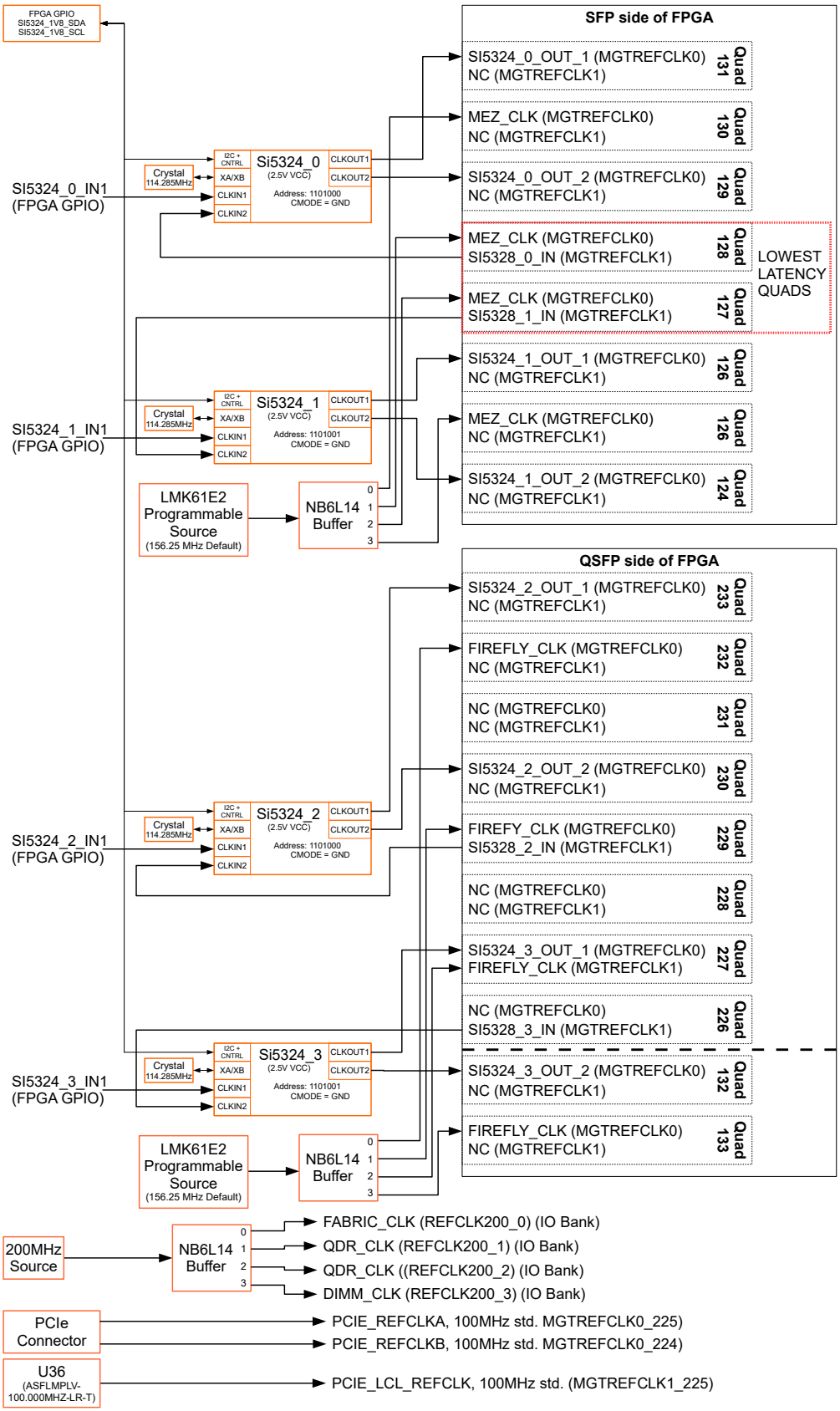

Figure 12 : Clock Topology

7.7.1 LMK61E2

The ADM-R9100 uses the LMK61E2 for arbitrary clock frequency synthesis. For complete technical details, please reference the datasheet:
https://www.ti.com/lit/ds/symlink/lmk61e2.pdf

The ADM-R9100 uses two LMK61E2 devices in the clock architecture. These can be accessed through either the USB or PCIe link using the AVR2UTIL application. See additional details on avr2util in the section: AD01474 System Monitor.

To re-program the LMK61E2 in a non-volatile manner, issue the following command:

```
avr2util <other options> setclknv-regmap <clock#> <reg. map file>
```

> **Note:**
> Each LMK61E2 is rated for only 100 non-volatile write operations.

To re-program the LMK61E2 in a volatile manner, issue the following command:

```
avr2util <other options> setclk-regmap <clock#> <reg. map file>
```

<other options> should be left blank for PCIE, and '-usbcom' for USB.

<clock#> is 0 for SFP clocks (nets MEZ_CLK*) and 1 for QSFP clocks (nets FIREFLY_CLK*).

<reg. map file> is a text file generated using the "LMK61xx Oscillator Programming Tool — SNAC074.ZIP" which can be obtained with a TI login from this page: https://www.ti.com/tool/LMK61E2EVM. After you have the tool installed, launch the application, type in the desired frequency, select "LVDS" output standard, click "Generate Configuration", then go to "File->Export hex register values".

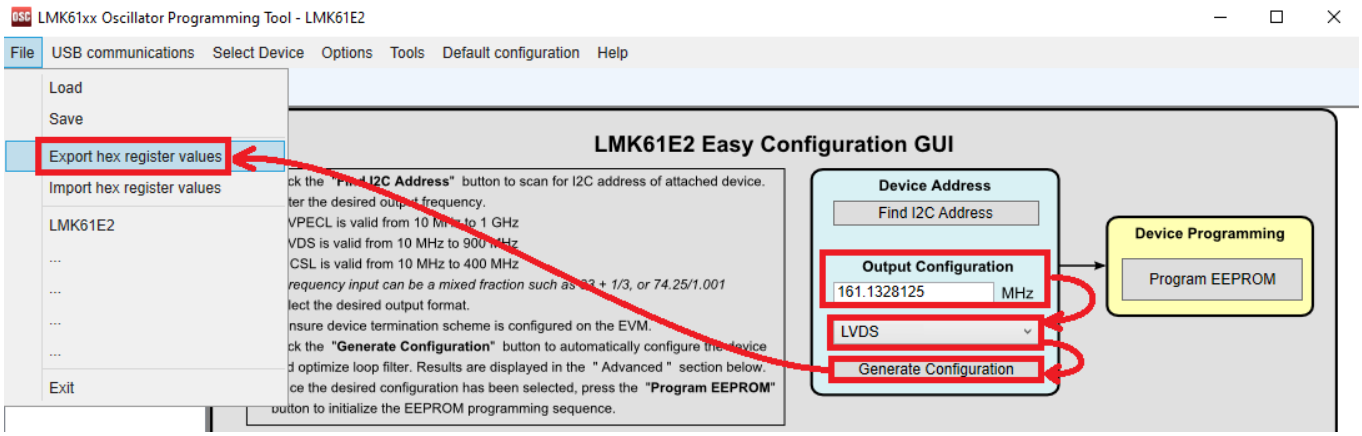

Figure 13 : LMK61xx Oscillator Programming Tool GUI

7.7.2 MGT Programable Clock

The MGT reference clocks connect quads throughout the device to ensure no quad is more than one tile north or south of a reference. This programable clock has a default 156.25MHz default. This clock frequency can be changed to any arbitrary clock frequency up to 900MHz by re-programming the LMK61E2 reprogrammable clock oscillator.

See net names MEZ_CLK_*_PIN_P/N and FIREFLY_CLK_*_PIN_P/N in the Complete AD01474 pinout for pin locations.

7.7.3 Si5324

Please note that some net names in the design refer to the SI5324 as an SI5328. These devices are footprint and functionally compatible. The SI5324E-C-GM was chosen at the time of production due to availability concerns and is the part fitted on every board. The Si5328 is not used.

If jitter attenuation is required please see the reference documentation for the Si5324.
www.skyworksinc.com/-/media/Skyworks/SL/documents/public/data-sheets/Si5324.pdf

There are two input clock options. Si5324 pin CLKIN1 (board net name SI5328_REFCLK_IN1_P/N) of the Si5324 is connected to a GPIO clock-capable pin, allowing the application design to feed this clock from anywhere within the FPGA PL. Si5324 pin CLKIN2 (board net name SI5328_*_CLKIN2_P/N) of the Si5324 is connected to an MGT clock output for the most direct clock recovery architecture.

The two output clocks are connected to different quads to provide clocking capability to all quads on the entire FPGA.

The INT_C1B and LOL signals for the Si5324 are available for use, and can be located at net names SI5328_*_INT_C1B and SI5328_*_LOL in the Complete AD01474 pinout.

The active low reset of the Si5324 is accessible to the FPGA. See net names SI5328_*_RST_L in the Complete AD01474 pinout.

Note:
INT_C1B and LOL have an external pull-up resistor.

Note:
SI5328_*_RST_L has a pull-down and will be reset when the FPGA is cleared.

The Si5328 configuration register map is volatile and must be written on each power-up event or FPGA reconfiguration over I2C. Use nets SI5328_SDA and SI5328_SCL at pins located in the Complete AD01474 pinout. The Si5324 devices are configured with the I2C addresses shown in the table below:

device	7bit Hex Address	Binary Address
Si5328_0	68	110_1000
Si5328_1	69	110_1001
Si5328_2	6A	110_1010
Si5328_3	6B	110_1011

Table 6 : Si5324 address table

7.7.4 PCIe Reference Clocks

The 8 MGT lanes connected to the SFF-8654 PCIe connector use the host system's 100 MHz PCIe reference clock (net name PCIE_REFCLKA_PIN_P/N or PCIE_REFCLKB_PIN_P/N_ in the Complete AD01474 pinout), where the "A" clock is primary.

Alternatively, a more stable but asynchronous onboard 100MHz clock is available as well (net name PCIE_LCL_REFCLK_P/N in the Complete AD01474 pinout).

7.7.5 REFCLK200

The design offers a 200MHz reference which is distributed to QDRII+, DDR4, and Global Clock-capable FPGA interface pins.

Use constraints IOSTANDARD LVDS for REFCLK200_0* and the Xilinx defaults for the memory interface clock constraints.

See net names REFCLK200_*_P/N in the Complete AD01474 pinout for pin locations.

7.8 Configuration

There are two main ways of configuring the FPGA on the ADM-R9100:

- From Flash memory, at power-on, as described in Section 7.8.1
- Using USB cable connected at either USB port Section 7.8.2

7.8.1 Configuration From Flash Memory

The FPGA can be automatically configured at power-on from a 1 Gbit QSPI flash memory device configured as an x4 SPI device (Micron part numbers MT25QU01GBBB8E12-0. This flash device is typically divided into two regions of 64 MiByte each, where each region is sufficiently large to hold an uncompressed bitstream for a VU2P FPGA.

The ADM-R9100 is shipped with a simple PCIe endpoint bitstream which should be visible to the operating system (using e.g. “lspci” in Linux) to provided confidence that the card is working correctly when installed in a system. On request, Alpha Data can pre-load custom bitstreams during the production test. Please contact sales@alpha-data.com to discuss this possibility.

It is possible to use Multiboot with a fallback image on this hardware. The master SPI configuration interface and the Fallback MultiBoot are discussed in detail in Xilinx UG570.

At power-on, the FPGA attempts to configure itself automatically in SPI master mode, depending on the header of the bitstream that has been flashed into the card. This normally results in SPIx4 configuration at EMCCLK frequency. The configuration scheme used in the ADM-R9100 is compatible with Multiboot; see Xilinx UG570 for details. The FPGA can also be made to reconfigure itself from an arbitrary Flash address using the ICAPE3 primitive; this is also described in Xilinx UG570.

The image loaded can also support tandem PROM or tandem PCIE with field update configuration methods. These options reduce power-on load times to help meet the PCIe reset timing requirements. Tandem with field update also enables a host system to reconfigure the user FPGA logic without losing the PCIe link, a useful feature when the system resets and power cycles are not an option.

The Alpha Data System Monitor is also capable of reconfiguring the flash memory and reprograming the FPGA. This provides a useful failsafe mechanism to re-program the FPGA even if it drops off the PCIe bus. The system monitor can be accessed with avr2util over USB at the front panel and rear edge.

7.8.1.1 Building and Programming Configuration Images

Generate a bit file with these constraints (see xapp1233):

- set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
- set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN {DIV-1} [current_design]
- set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
- set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
- set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
- set_property BITSTREAM.CONFIG.UNUSEDPIN {Pullnone} [current_design]
- set_property CFGBVS GND [current_design]
- set_property CONFIG_VOLTAGE 1.8 [current_design]
- set_property BITSTREAM.CONFIG.OVERTEMPSHUTDOWN Enable [current_design]

Generate an MCS file with these properties (write_cfgmem):

- -format MCS
- -size 128
- -interface SPIx4
- -loadbit "up 0x0000000 <directory/to/file/filename.bit>" (0th location)

Program with Vivado Hardware Manager with these settings (see xapp1233):

- SPI part: mt25qu01g-spi-x1_x2_x4
- State of non-config mem I/O pins: Pull-none

7.8.2 Configuration via JTAG

A micro-USB AB Cable may be attached to the front panel or rear edge USB port. This permits the FPGA to be reconfigured using the Xilinx Vivado Hardware Manager via the integrated Digilent JTAG converter box. The device will be automatically recognized in Vivado Hardware Manager.

For more detailed instructions, please see “Using a Vivado Hardware Manager to Program an FPGA Device” section of Xilinx UG908.

An example of this is shown in section: Using Vivado Lab to program the AD01474.

7.9 DDR4 SDRAM SODIMM

One bank of DDR4 SDRAM memory is available on a SODIMM within the FPGA board. The available density of the memory is 16GB. The memory interface is 72-bit wide data (64 data + 8 ECC). The maximum signaling rate is 2666 MT/s.

Memory solutions are available from the Xilinx Memory Interface Generator (MIG) tool. All pin location information is included in Complete AD01474 pinout.

The SODIMM part number fitted is MTA9ASF2G72HZ-3G2 or equivalent.

7.10 QDRII+

Two banks of QDRII+ memory are available on the FPGA board. Each bank has a 288Mb density. Each QDRII+ interface is comprised of two memory interfaces, each of 16-bit wide data (16Q and 16D bits). The maximum signaling rate is 550MHz.

Memory solutions are available from the Xilinx Memory Interface Generator (MIG) tool. All pin location information is included in Complete AD01474 pinout.

The QDRII+ part number fitted is CY7C2663KV18-550BZXC or equivalent.

8 System Monitoring

System monitor values can be read out from two places mainly: the AD01474 board and the CPU system (through ROMED4ID-2T's BMC).

8.1 AD01474 System Monitor

The ADA-R9100's USB connections described in the previous section can be used to directly access the system monitor system on the AD01474. All voltages, currents, temperatures, and non-volatile clock configuration settings can be accessed using Alpha Data's avr2util software at this interface (preinstalled in the Ubuntu OS).

Concerning the board health, the AD01474 monitors these temperatures, voltages, and currents in real-time. This information can be read out via USB using the avr2util utility as follows:

```
sudo avr2util-s -usbcom /dev/ttyACM0 display-sensors
```

You might need to add avr2util-s to the path if running it for the first time. Run the following if so:

```
sudo ln -s /home/ubuntu/avr2util-s-4.19.0/avr2util-s /usr/local/bin/avr2util-s
```

If the core FPGA temperature exceeds 105 degrees Celsius, the FPGA image will be cleared to prevent damage to the card.

Monitors	Identifier	Purpose/Description
ETC	ETC	Elapsed time counter (seconds)
EC	EC	Event counter (power cycles)
12V_DIG	ADC00	12V board input supply from 8-pin ATX Cable
12V_DIG_I	ADC01	12V board input current from 8-pin ATX Cable in amps
3V3_AUX	ADC02	3.3V auxiliary board input supply from 4-pin CPU cable (5VSB)
3V3_AUX_I	ADC03	3.3V auxiliary board input current from 4-pin CPU Cable in amps
3V3_DIG	ADC04	3.3V generated onboard for some circuits
2V5_DIG	ADC05	2.5V generated onboard for FPGA IO voltage (VCCO)
1V8_DIG	ADC06	1.8V generated onboard for FPGA IO voltage (VCCO)
1V8_DIG	ADC07	1.8V generated onboard for MGT Aux voltage
1V5_DIG	ADC08	1.5V generated onboard for FPGA IO voltage (VCCO)
1V2_DIG	ADC09	1.2V generated onboard for SDRAM and FPGA (VCCO)
1V2_AVTT	ADC10	1.2V generated onboard for transceiver Power (AVTT)
0V88_AVCC	ADC11	0.88V generated onboard for transceiver Power (AVCC)
VCC_INT	ADC12	0.8V generated onboard for FPGA core
0V6_VTT	ADC13	0.6V generated onboard for off-board SDRAM
uC_Temp	TMP00	uC on-die temperature
Board0_Temp	TMP01	Board temperature on-board 1
Board1_Temp	TMP02	Board temperature on-board 2
FPGA_Temp	TMP03	FPGA on-die temperature

Table 7 : Voltage, Current, and Temperature Monitors

To see all options use this command:

```
avr2util-s /?
```

8.1.1 System Monitor Status LEDs

LEDs D35 (Red) and D34 (Green) indicate the card health status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	FPGA configuration cleared to protect board

Table 8 : Status LED Definitions

8.2 BMC System Monitor

The CPU system centralises the readings of most of the system sensors, including AD01474 FPGA's temperature sensor (TR1), RPSU sensors through PMBus, etc ...

Monitors	Purpose/Description
Discrete	
ChassisIntr	chassis intrusion event (not available)
CPU_PROCHOT	processor too hot event
CPU_THERMTRIP	shutdown after processor too hot event
CPU_MCE	processor Machine Check Event (ECC/cache/bus error etc...)
Voltage	
VCPU	-
VSOC	-
VCCM ABCD	-
VCCM EFGH	-
VPPM ABCD	-
VPPM EFGH	-
3VSB	3.3V standby
5VSB	5V standby
1.8VSB	1.8V standby
1.8V	1.8V rail
BAT	battery voltage
3V	full-power 3V rail
5V	full-power 5V rail

Table 9 : Monitor groups accessible through BMC (continued on next page)

Voltage	
VCPU	-
12V	full-power 12V rail
LAN_1.2V	Ethernet chipset voltage 1
LAN_0.83V	Ethernet chipset voltage 1
Temperatures (degrees Celsius)	
CPU Temp	CPU on-die temperature
MB Temp	Motherboard chipset temperature
TR1 Temp	AD01474 FPGA on-die temperature
DDR4_C Temp	DDR4 ECC module temperature
PSU1 Temp	RPSU Module 1 temperature
PSU2 Temp	RPSU Module 2 temperature
Fan speeds (RPM)	
FAN1	AD01474 fan array speed
FAN3	ROMED4ID-2T CPU fan array speed
Voltage (Volts)	
PSU1 VIN	RPSU Module 1 input voltage (AC)
PSU2 VIN	RPSU Module 2 input voltage (AC)
Current (Amps)	
PSU1 IOUT	RPSU Module 1 input current (AC)
PSU2 IOUT	RPSU Module 2 input current (AC)
Power (Watts)	
CPU Power	ROMED4ID-2T's CPU power
PSU1 PIN	RPSU Module 1 input power
PSU2 PIN	RPSU Module 2 input power
PSU1 POUT	RPSU Module 1 output power
PSU2 POUT	RPSU Module 2 output power
Discrete	
PSU1 Status	RPSU Module 1 presence detection
PSU2 Status	RPSU Module 2 presence detection
PSU1 AC lost	RPSU Module 1 VAC input disconnected
PSU2 AC lost	RPSU Module 2 VAC input disconnected

Table 9 : Monitor groups accessible through BMC

To read out information from these sensors, refer to Section Section 10 for GUI access and Section 11.2 for command-line access.

9 Using Vivado Lab to program the AD01474

Once the system is powered up and has booted into Ubuntu, the default user credentials must be provided to log into Ubuntu through its GUI.

Go to "Activities" and type Vivado, then you can right-click on Vivado's icon to add it to favourites for easy access next time:

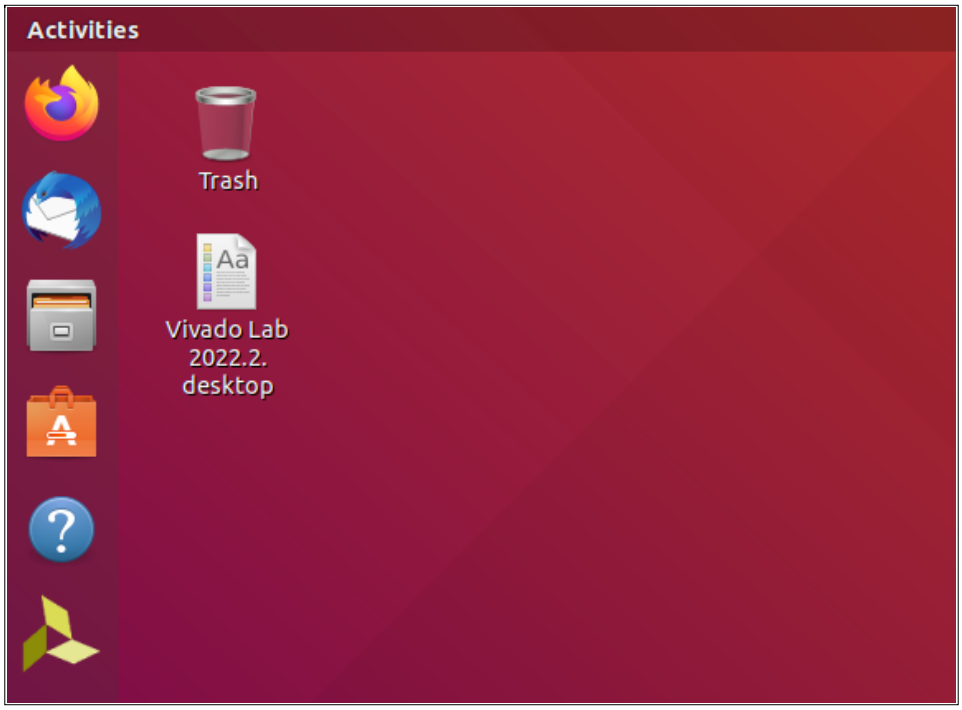

Figure 14 : Adding Vivado 2022.2 to favourites in Ubuntu GUI

Click on the icon to open Vivado:

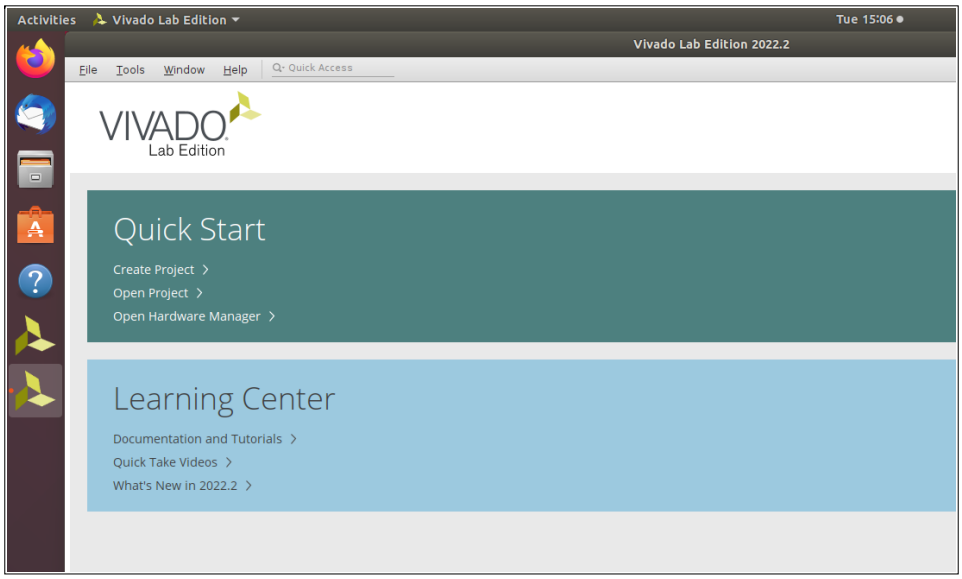

Figure 15 : Opening Vivado 2022.2 in Ubuntu GUI

Click "Open Hardware Manager" in the Quick Start menu:

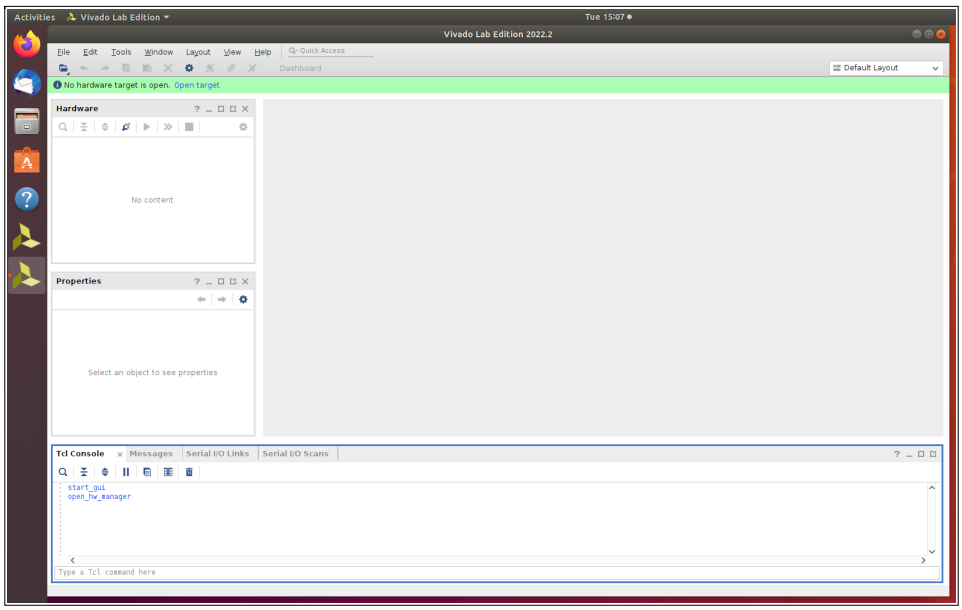

Figure 16 : Opening HW Manager

Click on the 'Open Target' button that appears at the top, then select 'Auto Connect.' The software will scan the JTAG chain for the FPGA and display its programming status upon detection. This occurs because the FPGA is automatically programmed with a default image from Flash during power-up. You can observe the multi-gigabit transceivers (MGT) appearing as operational components on the FPGA. These are mapped to the physical connections on the SFP+/QSFP28 boards.

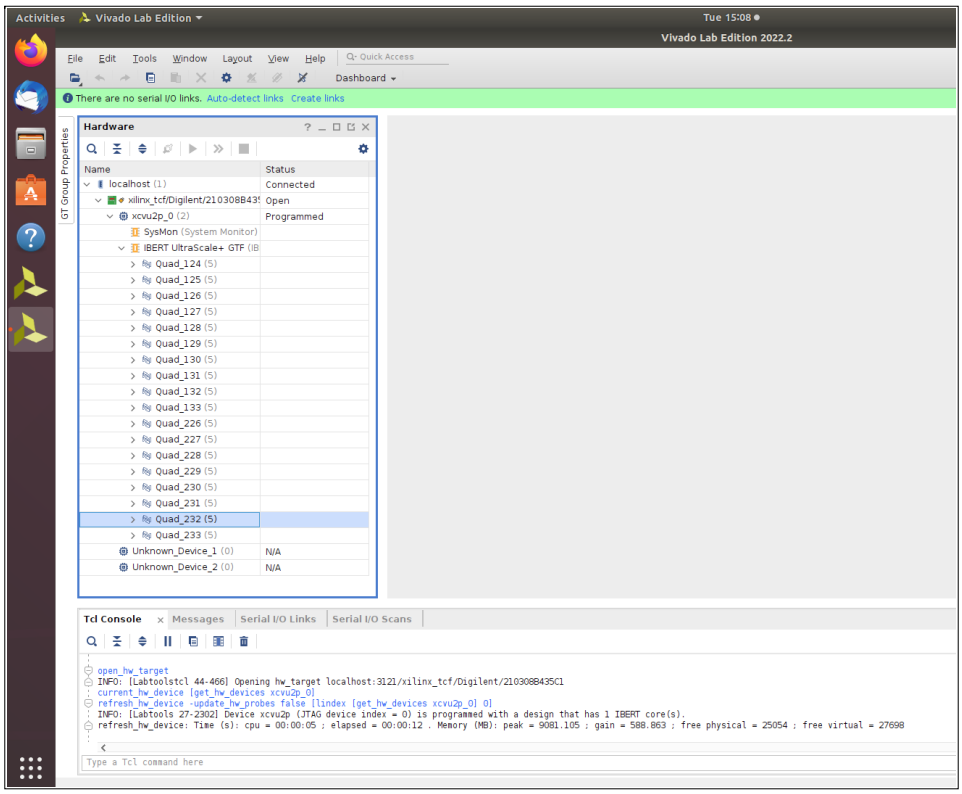

Figure 17 : Scanning the JTAG chain for the FPGA

Right click on the FPGA part number detected on the JTAG chain (XCVU2P) and click "Program" to reprogram the FPGA with a different bitstream if needed:

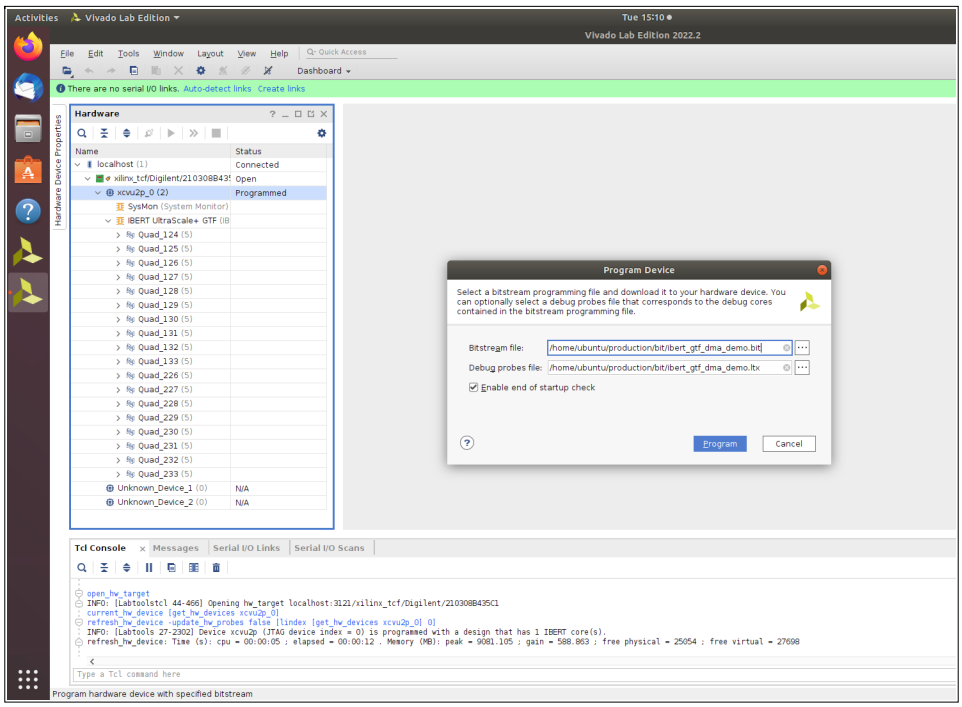

Figure 18 : Reprogramming the FPGA

Note:
Example designs are available for this system. You can request them at support@alpha-data.com.

10 Management interface (BMC)

The BMC processor provides the server capabilities to the system addresses, managing the different services and subsystems. The R9100 is configured to get IP adressess for the BMC and the CPU system automatically. In order to gain access to the system, the assigned IP address by your DHCP server is needed. It is assumed that network cables have been connected to both network interfaces (see Section 3, items 9 and 12).

First up, connect a monitor to the R9100's VGA port (Section 3, item 10). Then, turn the system ON or press "Reset" if it was already ON (Section 3, item 2).

You should see the system booting up, and BMC's IP address shown on the screen before the BIOS screen (and during it once again):

Figure 19 : Getting BMC IP at boot

10.1 Remote access through BMC (Web)

Now that we know the BMC's IP address, open a browser from a computer on the same network and introduce the obtained IP address to access the HTTP server of the BMC:

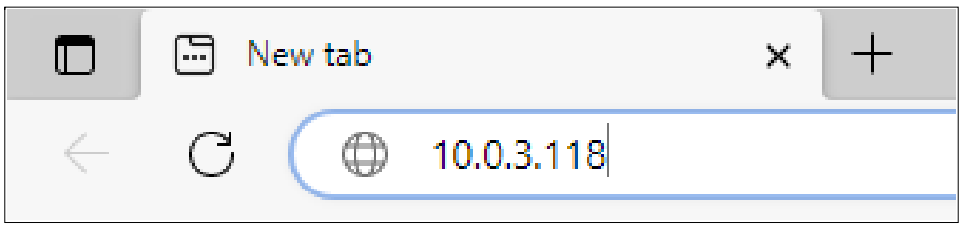

Figure 20 : Accessing BMC's HTTP server

The BMC login screen will pop up. You will need to provide here the default administrator account credentials:

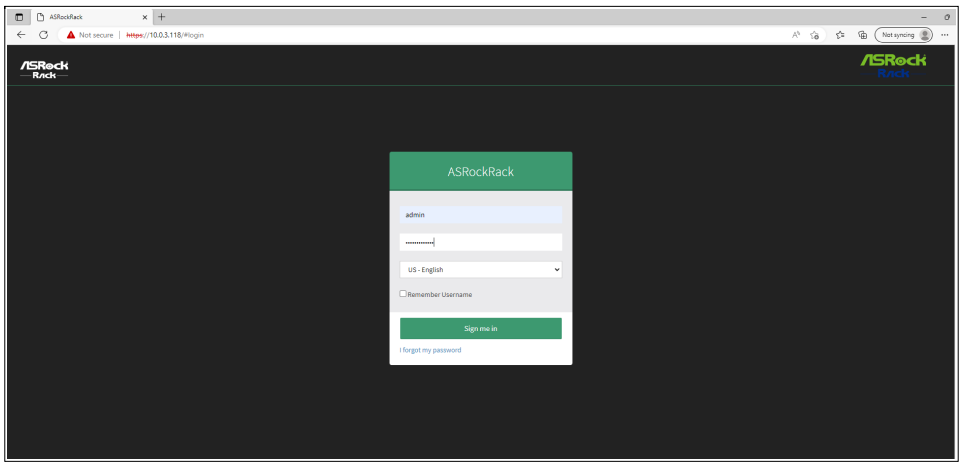

Figure 21 : BMC's administrator login

You will be able to browse through the BMC's different options. See the sensors list below:

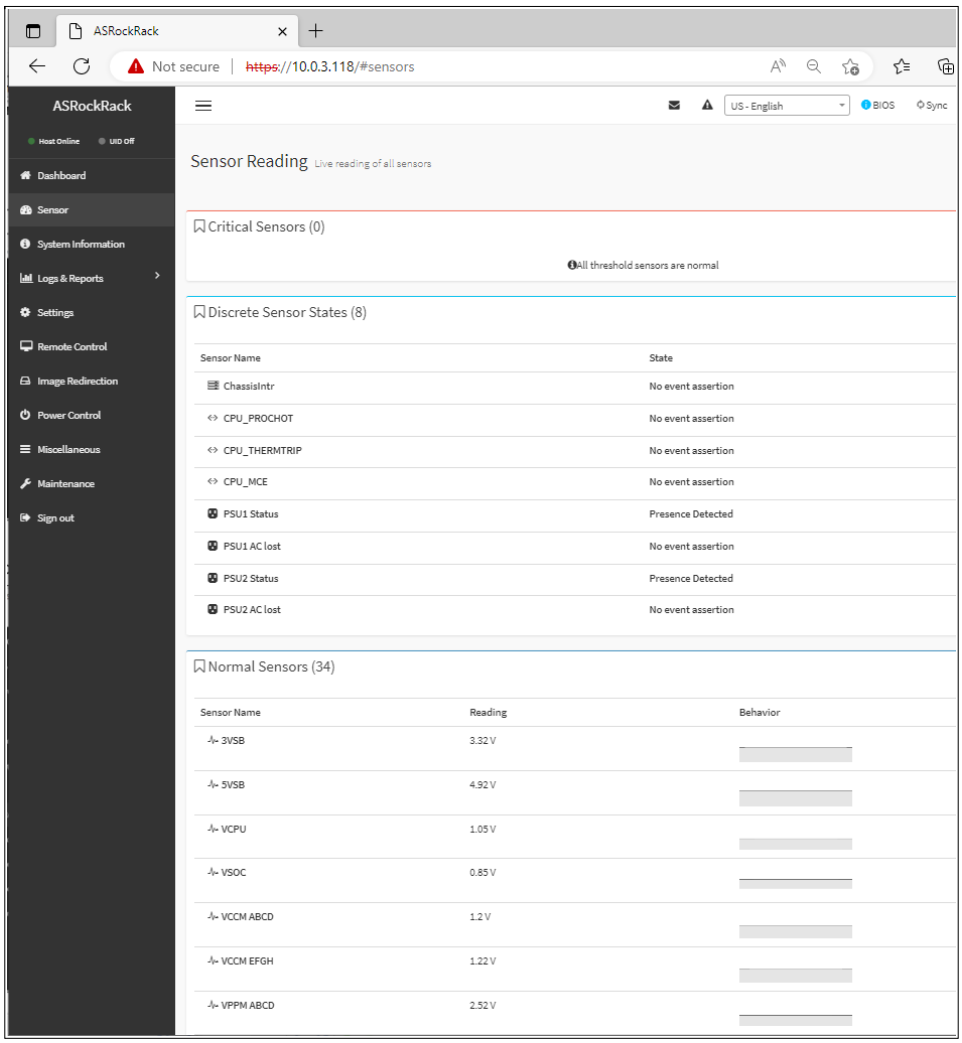

Figure 22 : BMC's sensors list

10.2 Remote connection to server (GUI)

Now, let us open the KVM options to remote control the CPU system. Click on "Remote Control" on the left options pane, and two options will appear on the screen. For ease of access, use the HTML-based viewer H5Viewer from the remote desktop:

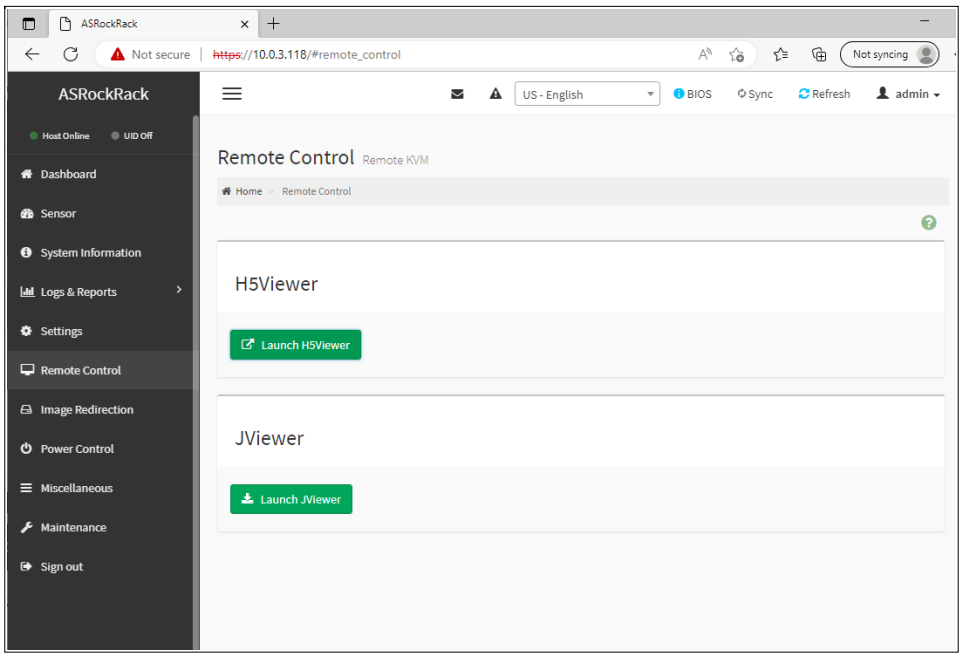

Figure 23 : KVM remote control

Next, the login screen of the CPU system (Ubuntu) will be displayed:

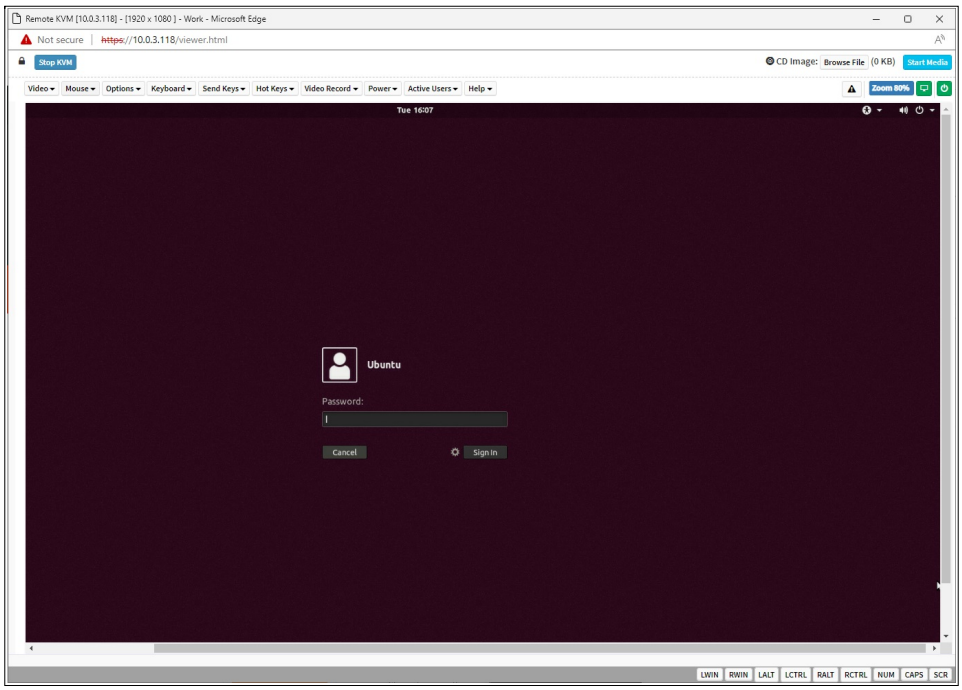

Figure 24 : Ubuntu through KVM

You can operate the system entirely from here, including performing an ACPI shutdown, reboot, etc. Then you can access the BIOS by pressing F2 or Del when prompted:

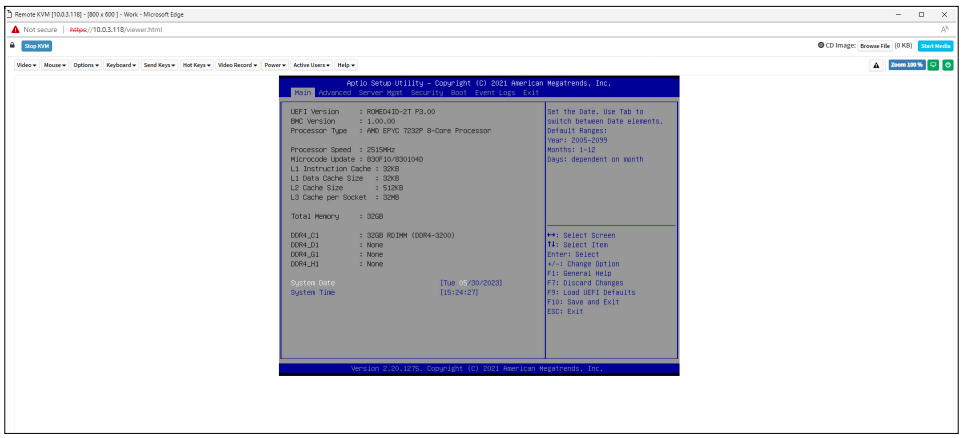

Figure 25 : Accessing system BIOS remotely

Note:
WARNING! The CPU on the ROMED4ID-2T has been preconfigured to run at **80%** of its maximum speed by default. This maximises the available power for the user application on the AD01474/75/76 subsystem and ensures the RPSU operating limits. This is after considering component derating curves and ADA-R9100's safety certification, which specifies a maximum operating temperature of 50 degrees Celsius. The CPU's speed **SHOULD NOT** be increased. Please contact support@alpha-data.com if this causes a problem for your application.

11 Remote Control and Monitoring through console commands (IPMI)

The main monitoring functions are carried out by ROMED4D-2T's BMC, and these can be accessed through the GUI (Figure 22) or queried with console commands. These are referred to as sensors in the BMC. For a complete list of accessible sensors see appendix System Sensors and Monitoring.

To monitor and control the R9100 remotely through console commands (scriptable), the**ipmitool** application (Linux) needs to be installed on the remote host.

> **Note:**
> Administrator privileges on the BMC are needed for most of the remote commands described here. Check permissions with the network administrator and/or request account permissions change on the BMC.

11.1 Turn chassis ON/OFF

To turn it on:

```
ipmitool -H <BMC_IP_address> -I lanplus -U <user> -P <password> chassis power on
```

To turn it off:

```
ipmitool -H <BMC_IP_address> -I lanplus -U <user> -P <password> chassis power off
```

11.2 GET Commands

The simplest way to get the readings of all the system sensors (BMC) is by running the following command:

```
ipmitool -H 10.0.3.118 -U user -P password -I lanplus sdr
```

Or locally:

```
ipmitool sdr
```

```
3VSB             | 3.40 Volts        | ok
5VSB             | 5.13 Volts        | ok
VCPU             | 1.12 Volts        | ok
VSOC             | 0.85 Volts        | ok
VCCM ABCD        | 1.21 Volts        | ok
VCCM EFGH        | 1.22 Volts        | ok
BAT              | 3.04 Volts        | ok
3V               | 3.32 Volts        | ok
5V               | 5.04 Volts        | ok
12V              | 12.30 Volts       | ok
MB Temp          | 32 degrees C      | ok ... (continues)
```

11.2.1 Get RPSU State

You can query for the RPSU monitored values by sensor name, i.e.: "PS1 POUT". Then, filter sensor reading:

```
ipmitool -H 10.0.3.118 -U user -P password -I lanplus sensor get "PSU1 POUT"
            | grep "Sensor Reading"
```

```
Sensor Reading        : 26 (± 0) Watts
```

Likewise, status registers are decoded when querying them (no need to filter for sensor values here):

```
ipmitool -H 10.0.3.118 -U user -P password -I lanplus sensor get "PSU2 Status"
```

```
Locating sensor record...
```

```
Sensor ID              : PSU2 Status (0xa8)
Entity ID             : 10.0
Sensor Type (Discrete): Power Supply
States Asserted       : Power Supply
[Presence detected]
```

Find below the list of RPSU sensors accessible with PMBus through the ROMED4ID-2T (PSUX=[PSU1|PSU2]):

Sensor Name	Output Value/s	Description
PSUX Status	Presence detected/ Not detected	module detected/not detected in its bay
PSUX AC lost	Power Supply Input Lost (AC/ DC)/ No event assertion	module disconnected from power lines
PSUX VIN	decimal value in Volts	input voltage measured at the input AC port
PSUX IOUT	decimal value in Amperes	output current measured at the DC output
PSUX Temp	decimal value in Degrees Celsius	temperature measured at redundant PSU module
PSUX PIN	decimal value in Watts	power consumption measured at the AC input of the redundant PSU module
PSUX POUT	decimal value in Watts	power consumption measured at the DC output of the redundant PSU module

Table 10 : System Status at Standby Power

You can find these sensors alongside the full sensor list in the System Sensors and Monitoring appendix.

Note:
These commands can be directly sent to the RPSU in raw format too. For an extended version of the command list, contact support@alpha-data.com

11.2.2 Get CPU temperature

Gets the instantaneous temperature value (in degrees Celsius) of the ROMED4ID-2T CPU's temperature sensor:

```
ipmitool -H 10.0.3.82 -U user -P password -I lanplus sensor get \"CPU Temp\" | grep
\"Sensor Reading\" | cut -c26-
```

11.2.3 Get FPGA temperature

Gets the instantaneous temperature value (in degrees Celsius) of the FPGA's temperature sensor of the AD01474:

```
ipmitool -H 10.0.3.82 -U user -P password -I lanplus sensor get \"TR1 Temp\" | grep
\"Sensor Reading\" | cut -c26-
```

11.2.4 Get Fan Array speeds

Gets the instantanous speed value in R.P.M. of the queried fan array section. The two implemented sections are:

FAN1 => AD01474
FAN3 => ROMED4ID-2T

To get their speeds, run the following command:

```
ipmitool -H 10.0.3.82 -U user -P password -I lanplus sensor get \"FAN1\" | grep \"
Sensor Reading\" | cut -c26-
```

11.3 SET Commands (IPMI raw)

11.3.1 Set chassis fan array speeds

Fan array speeds are set independently for ROMED4ID-2T and AD01474 to handle their cooling, with two arrays of x3 fans each (Figure 2). The R9100 is set to run in auto mode, and each part of the array is based on tabulated duty cycles for each of the subsystem requirements.

> **Note:**
> **WARNING!** The commands below will override automatic mode. This can cause damage to the system. Please contact support@alpha-data.com if there are problems restoring manufacturing values.Section 11.3.4

11.3.2 Set fans to manual mode

As discussed above, each section of the fan array corresponds to a subsystem:

FAN1 => AD01474
FAN3 => ROMED4ID-2T

To set both modes to manual, run the following command:

```
#Fan modes: FAN1,FAN2,FAN3=(Manual,Default,Manual)
```

```
ipmitool -H 10.0.3.82 -U user -P password -I lanplus raw 0x3a 0xd8 0x01 0x00 0x01
0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
```

11.3.3 Set fan speed

This commmand sets a fixed speed on the fans based on a duty cycle value. It ranges from 20% to 100% duty cycle (0x14/ 0x64 in hexadecimal, as required by the command)

```
ipmitool -H 10.0.3.82 -U user -P password -I lanplus raw 0x3a 0xd6 0xXX 0x14 0xYY
0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14
```

where:

XX => FAN1 duty => AD01474
YY => FAN3 duty => ROMED4ID-2T

> **Note:**
> The command needs to be padded with additional speeds that are not used (0x14 0x14 ...)

Setting the fans to minimum speed:

```
ipmitool -H 10.0.3.82 -U user -P password -I lanplus raw 0x3a 0xd6 0x14 0x14 0x14
0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14
```

Setting the fans to maximum speed:

```
ipmitool -H 10.0.3.82 -U user -P password -I lanplus raw 0x3a 0xd6 0x64 0x64 0x64
0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14 0x14
```

11.3.4 Set fans to auto mode

To set speeds to auto mode and effectively return to the default manufacturer levels (provided duty cycle/temp tables and their assignment have not been changed), set the fan settings to **custom** and **default** respectively:

(FAN1: customized, FAN2/3: default)

```
ipmitool -H 10.0.3.82 -U user -P password -I lanplus raw 0x3a 0xd8 0x02 0x00 0x00
0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
```

Appendix A: Complete AD01474 pinout

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
AK3	MGTFRXN0_227	FIREFLY_6_RX0_N	MGT	J3B1
AK4	MGTFRXP0_227	FIREFLY_6_RX0_P	MGT	J3B1
AJ1	MGTFRXN1_227	FIREFLY_6_RX1_N	MGT	J3B1
AJ2	MGTFRXP1_227	FIREFLY_6_RX1_P	MGT	J3B1
AH3	MGTFRXN2_227	FIREFLY_6_RX2_N	MGT	J3B1
AH4	MGTFRXP2_227	FIREFLY_6_RX2_P	MGT	J3B1
AG1	MGTFRXN3_227	FIREFLY_6_RX3_N	MGT	J3B1
AG2	MGTFRXP3_227	FIREFLY_6_RX3_P	MGT	J3B1
AM8	MGTFTXN0_227	FIREFLY_6_TX0_N	MGT	J3B1
AM9	MGTFTXP0_227	FIREFLY_6_TX0_P	MGT	J3B1
AL6	MGTFTXN1_227	FIREFLY_6_TX1_N	MGT	J3B1
AL7	MGTFTXP1_227	FIREFLY_6_TX1_P	MGT	J3B1
AK8	MGTFTXN2_227	FIREFLY_6_TX2_N	MGT	J3B1
AK9	MGTFTXP2_227	FIREFLY_6_TX2_P	MGT	J3B1
AJ6	MGTFTXN3_227	FIREFLY_6_TX3_N	MGT	J3B1
AJ7	MGTFTXP3_227	FIREFLY_6_TX3_P	MGT	J3B1
AF3	MGTFRXN0_228	FIREFLY_5_RX0_N	MGT	J3B2
AF4	MGTFRXP0_228	FIREFLY_5_RX0_P	MGT	J3B2
AE1	MGTFRXN1_228	FIREFLY_5_RX1_N	MGT	J3B2
AE2	MGTFRXP1_228	FIREFLY_5_RX1_P	MGT	J3B2
AD3	MGTFRXN2_228	FIREFLY_5_RX2_N	MGT	J3B2
AD4	MGTFRXP2_228	FIREFLY_5_RX2_P	MGT	J3B2
AC1	MGTFRXN3_228	FIREFLY_5_RX3_N	MGT	J3B2
AC2	MGTFRXP3_228	FIREFLY_5_RX3_P	MGT	J3B2
AH8	MGTFTXN0_228	FIREFLY_5_TX0_N	MGT	J3B2
AH9	MGTFTXP0_228	FIREFLY_5_TX0_P	MGT	J3B2
AG6	MGTFTXN1_228	FIREFLY_5_TX1_N	MGT	J3B2
AG7	MGTFTXP1_228	FIREFLY_5_TX1_P	MGT	J3B2
AF8	MGTFTXN2_228	FIREFLY_5_TX2_N	MGT	J3B2
AF9	MGTFTXP2_228	FIREFLY_5_TX2_P	MGT	J3B2
AE6	MGTFTXN3_228	FIREFLY_5_TX3_N	MGT	J3B2
AE7	MGTFTXP3_228	FIREFLY_5_TX3_P	MGT	J3B2

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
AB3	MGTFRXN0_229	FIREFLY_3_RX0_N	MGT	J3B3
AB4	MGTFRXP0_229	FIREFLY_3_RX0_P	MGT	J3B3
AA1	MGTFRXN1_229	FIREFLY_3_RX1_N	MGT	J3B3
AA2	MGTFRXP1_229	FIREFLY_3_RX1_P	MGT	J3B3
Y3	MGTFRXN2_229	FIREFLY_3_RX2_N	MGT	J3B3
Y4	MGTFRXP2_229	FIREFLY_3_RX2_P	MGT	J3B3
W1	MGTFRXN3_229	FIREFLY_3_RX3_N	MGT	J3B3
W2	MGTFRXP3_229	FIREFLY_3_RX3_P	MGT	J3B3
AD8	MGTFTXN0_229	FIREFLY_3_TX0_N	MGT	J3B3
AD9	MGTFTXP0_229	FIREFLY_3_TX0_P	MGT	J3B3
AC6	MGTFTXN1_229	FIREFLY_3_TX1_N	MGT	J3B3
AC7	MGTFTXP1_229	FIREFLY_3_TX1_P	MGT	J3B3
AB8	MGTFTXN2_229	FIREFLY_3_TX2_N	MGT	J3B3
AB9	MGTFTXP2_229	FIREFLY_3_TX2_P	MGT	J3B3
AA6	MGTFTXN3_229	FIREFLY_3_TX3_N	MGT	J3B3
AA7	MGTFTXP3_229	FIREFLY_3_TX3_P	MGT	J3B3
K3	MGTFRXN0_232	FIREFLY_1_RX0_N	MGT	J3B4
K4	MGTFRXP0_232	FIREFLY_1_RX0_P	MGT	J3B4
J1	MGTFRXN1_232	FIREFLY_1_RX1_N	MGT	J3B4
J2	MGTFRXP1_232	FIREFLY_1_RX1_P	MGT	J3B4
H3	MGTFRXN2_232	FIREFLY_1_RX2_N	MGT	J3B4
H4	MGTFRXP2_232	FIREFLY_1_RX2_P	MGT	J3B4
G1	MGTFRXN3_232	FIREFLY_1_RX3_N	MGT	J3B4
G2	MGTFRXP3_232	FIREFLY_1_RX3_P	MGT	J3B4
M8	MGTFTXN0_232	FIREFLY_1_TX0_N	MGT	J3B4
M9	MGTFTXP0_232	FIREFLY_1_TX0_P	MGT	J3B4
L6	MGTFTXN1_232	FIREFLY_1_TX1_N	MGT	J3B4
L7	MGTFTXP1_232	FIREFLY_1_TX1_P	MGT	J3B4
K8	MGTFTXN2_232	FIREFLY_1_TX2_N	MGT	J3B4
K9	MGTFTXP2_232	FIREFLY_1_TX2_P	MGT	J3B4
J6	MGTFTXN3_232	FIREFLY_1_TX3_N	MGT	J3B4
J7	MGTFTXP3_232	FIREFLY_1_TX3_P	MGT	J3B4
K44	MGTFRXN0_132	FIREFLY_8_RX0_N	MGT	J3B5
K43	MGTFRXP0_132	FIREFLY_8_RX0_P	MGT	J3B5
J46	MGTFRXN1_132	FIREFLY_8_RX1_N	MGT	J3B5

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
J45	MGTFRXP1_132	FIREFLY_8_RX1_P	MGT	J3B5
H44	MGTFRXN2_132	FIREFLY_8_RX2_N	MGT	J3B5
H43	MGTFRXP2_132	FIREFLY_8_RX2_P	MGT	J3B5
G46	MGTFRXN3_132	FIREFLY_8_RX3_N	MGT	J3B5
G45	MGTFRXP3_132	FIREFLY_8_RX3_P	MGT	J3B5
M39	MGTFTXN0_132	FIREFLY_8_TX0_N	MGT	J3B5
M38	MGTFTXP0_132	FIREFLY_8_TX0_P	MGT	J3B5
L41	MGTFTXN1_132	FIREFLY_8_TX1_N	MGT	J3B5
L40	MGTFTXP1_132	FIREFLY_8_TX1_P	MGT	J3B5
K39	MGTFTXN2_132	FIREFLY_8_TX2_N	MGT	J3B5
K38	MGTFTXP2_132	FIREFLY_8_TX2_P	MGT	J3B5
J41	MGTFTXN3_132	FIREFLY_8_TX3_N	MGT	J3B5
J40	MGTFTXP3_132	FIREFLY_8_TX3_P	MGT	J3B5
AP3	MGTFRXN0_226	FIREFLY_7_RX0_N	MGT	J3T1
AP4	MGTFRXP0_226	FIREFLY_7_RX0_P	MGT	J3T1
AN1	MGTFRXN1_226	FIREFLY_7_RX1_N	MGT	J3T1
AN2	MGTFRXP1_226	FIREFLY_7_RX1_P	MGT	J3T1
AM3	MGTFRXN2_226	FIREFLY_7_RX2_N	MGT	J3T1
AM4	MGTFRXP2_226	FIREFLY_7_RX2_P	MGT	J3T1
AL1	MGTFRXN3_226	FIREFLY_7_RX3_N	MGT	J3T1
AL2	MGTFRXP3_226	FIREFLY_7_RX3_P	MGT	J3T1
AT8	MGTFTXN0_226	FIREFLY_7_TX0_N	MGT	J3T1
AT9	MGTFTXP0_226	FIREFLY_7_TX0_P	MGT	J3T1
AR6	MGTFTXN1_226	FIREFLY_7_TX1_N	MGT	J3T1
AR7	MGTFTXP1_226	FIREFLY_7_TX1_P	MGT	J3T1
AP8	MGTFTXN2_226	FIREFLY_7_TX2_N	MGT	J3T1
AP9	MGTFTXP2_226	FIREFLY_7_TX2_P	MGT	J3T1
AN6	MGTFTXN3_226	FIREFLY_7_TX3_N	MGT	J3T1
AN7	MGTFTXP3_226	FIREFLY_7_TX3_P	MGT	J3T1
V3	MGTFRXN0_230	FIREFLY_4_RX0_N	MGT	J3T2
V4	MGTFRXP0_230	FIREFLY_4_RX0_P	MGT	J3T2
U1	MGTFRXN1_230	FIREFLY_4_RX1_N	MGT	J3T2
U2	MGTFRXP1_230	FIREFLY_4_RX1_P	MGT	J3T2
T3	MGTFRXN2_230	FIREFLY_4_RX2_N	MGT	J3T2
T4	MGTFRXP2_230	FIREFLY_4_RX2_P	MGT	J3T2

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
R1	MGTFRXN3_230	FIREFLY_4_RX3_N	MGT	J3T2
R2	MGTFRXP3_230	FIREFLY_4_RX3_P	MGT	J3T2
Y8	MGTFTXN0_230	FIREFLY_4_TX0_N	MGT	J3T2
Y9	MGTFTXP0_230	FIREFLY_4_TX0_P	MGT	J3T2
W6	MGTFTXN1_230	FIREFLY_4_TX1_N	MGT	J3T2
W7	MGTFTXP1_230	FIREFLY_4_TX1_P	MGT	J3T2
V8	MGTFTXN2_230	FIREFLY_4_TX2_N	MGT	J3T2
V9	MGTFTXP2_230	FIREFLY_4_TX2_P	MGT	J3T2
U6	MGTFTXN3_230	FIREFLY_4_TX3_N	MGT	J3T2
U7	MGTFTXP3_230	FIREFLY_4_TX3_P	MGT	J3T2
P3	MGTFRXN0_231	FIREFLY_2_RX0_N	MGT	J3T3
P4	MGTFRXP0_231	FIREFLY_2_RX0_P	MGT	J3T3
N1	MGTFRXN1_231	FIREFLY_2_RX1_N	MGT	J3T3
N2	MGTFRXP1_231	FIREFLY_2_RX1_P	MGT	J3T3
M3	MGTFRXN2_231	FIREFLY_2_RX2_N	MGT	J3T3
M4	MGTFRXP2_231	FIREFLY_2_RX2_P	MGT	J3T3
L1	MGTFRXN3_231	FIREFLY_2_RX3_N	MGT	J3T3
L2	MGTFRXP3_231	FIREFLY_2_RX3_P	MGT	J3T3
T8	MGTFTXN0_231	FIREFLY_2_TX0_N	MGT	J3T3
T9	MGTFTXP0_231	FIREFLY_2_TX0_P	MGT	J3T3
R6	MGTFTXN1_231	FIREFLY_2_TX1_N	MGT	J3T3
R7	MGTFTXP1_231	FIREFLY_2_TX1_P	MGT	J3T3
P8	MGTFTXN2_231	FIREFLY_2_TX2_N	MGT	J3T3
P9	MGTFTXP2_231	FIREFLY_2_TX2_P	MGT	J3T3
N6	MGTFTXN3_231	FIREFLY_2_TX3_N	MGT	J3T3
N7	MGTFTXP3_231	FIREFLY_2_TX3_P	MGT	J3T3
F3	MGTFRXN0_233	FIREFLY_0_RX0_N	MGT	J3T4
F4	MGTFRXP0_233	FIREFLY_0_RX0_P	MGT	J3T4
E1	MGTFRXN1_233	FIREFLY_0_RX1_N	MGT	J3T4
E2	MGTFRXP1_233	FIREFLY_0_RX1_P	MGT	J3T4
D3	MGTFRXN2_233	FIREFLY_0_RX2_N	MGT	J3T4
D4	MGTFRXP2_233	FIREFLY_0_RX2_P	MGT	J3T4
B3	MGTFRXN3_233	FIREFLY_0_RX3_N	MGT	J3T4
B4	MGTFRXP3_233	FIREFLY_0_RX3_P	MGT	J3T4
G6	MGTFTXN0_233	FIREFLY_0_TX0_N	MGT	J3T4

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
G7	MGTFTXP0_233	FIREFLY_0_TX0_P	MGT	J3T4
E6	MGTFTXN1_233	FIREFLY_0_TX1_N	MGT	J3T4
E7	MGTFTXP1_233	FIREFLY_0_TX1_P	MGT	J3T4
C6	MGTFTXN2_233	FIREFLY_0_TX2_N	MGT	J3T4
C7	MGTFTXP2_233	FIREFLY_0_TX2_P	MGT	J3T4
A6	MGTFTXN3_233	FIREFLY_0_TX3_N	MGT	J3T4
A7	MGTFTXP3_233	FIREFLY_0_TX3_P	MGT	J3T4
F44	MGTFRXN0_133	FIREFLY_9_RX0_N	MGT	J3T5
F43	MGTFRXP0_133	FIREFLY_9_RX0_P	MGT	J3T5
E46	MGTFRXN1_133	FIREFLY_9_RX1_N	MGT	J3T5
E45	MGTFRXP1_133	FIREFLY_9_RX1_P	MGT	J3T5
D44	MGTFRXN2_133	FIREFLY_9_RX2_N	MGT	J3T5
D43	MGTFRXP2_133	FIREFLY_9_RX2_P	MGT	J3T5
B44	MGTFRXN3_133	FIREFLY_9_RX3_N	MGT	J3T5
B43	MGTFRXP3_133	FIREFLY_9_RX3_P	MGT	J3T5
G41	MGTFTXN0_133	FIREFLY_9_TX0_N	MGT	J3T5
G40	MGTFTXP0_133	FIREFLY_9_TX0_P	MGT	J3T5
E41	MGTFTXN1_133	FIREFLY_9_TX1_N	MGT	J3T5
E40	MGTFTXP1_133	FIREFLY_9_TX1_P	MGT	J3T5
C41	MGTFTXN2_133	FIREFLY_9_TX2_N	MGT	J3T5
C40	MGTFTXP2_133	FIREFLY_9_TX2_P	MGT	J3T5
A41	MGTFTXN3_133	FIREFLY_9_TX3_N	MGT	J3T5
A40	MGTFTXP3_133	FIREFLY_9_TX3_P	MGT	J3T5
BC46	MGTFRXN0_124	MGT_124_RX0_N	MGT	J4B1
BC45	MGTFRXP0_124	MGT_124_RX0_P	MGT	J4B1
BF43	MGTFTXN0_124	MGT_124_TX0_N	MGT	J4B1
BF42	MGTFTXP0_124	MGT_124_TX0_P	MGT	J4B1
AD44	MGTFRXN2_128	MGT_128_RX2_N	MGT	J4B10
AD43	MGTFRXP2_128	MGT_128_RX2_P	MGT	J4B10
AF39	MGTFTXN2_128	MGT_128_TX2_N	MGT	J4B10
AF38	MGTFTXP2_128	MGT_128_TX2_P	MGT	J4B10
AB44	MGTFRXN0_129	MGT_129_RX0_N	MGT	J4B11
AB43	MGTFRXP0_129	MGT_129_RX0_P	MGT	J4B11
AD39	MGTFTXN0_129	MGT_129_TX0_N	MGT	J4B11
AD38	MGTFTXP0_129	MGT_129_TX0_P	MGT	J4B11

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
Y44	MGTFRXN2_129	MGT_129_RX2_N	MGT	J4B12
Y43	MGTFRXP2_129	MGT_129_RX2_P	MGT	J4B12
AB39	MGTFTXN2_129	MGT_129_TX2_N	MGT	J4B12
AB38	MGTFTXP2_129	MGT_129_TX2_P	MGT	J4B12
V44	MGTFRXN0_130	MGT_130_RX0_N	MGT	J4B13
V43	MGTFRXP0_130	MGT_130_RX0_P	MGT	J4B13
Y39	MGTFTXN0_130	MGT_130_TX0_N	MGT	J4B13
Y38	MGTFTXP0_130	MGT_130_TX0_P	MGT	J4B13
T44	MGTFRXN2_130	MGT_130_RX2_N	MGT	J4B14
T43	MGTFRXP2_130	MGT_130_RX2_P	MGT	J4B14
V39	MGTFTXN2_130	MGT_130_TX2_N	MGT	J4B14
V38	MGTFTXP2_130	MGT_130_TX2_P	MGT	J4B14
P44	MGTFRXN0_131	MGT_131_RX0_N	MGT	J4B15
P43	MGTFRXP0_131	MGT_131_RX0_P	MGT	J4B15
T39	MGTFTXN0_131	MGT_131_TX0_N	MGT	J4B15
T38	MGTFTXP0_131	MGT_131_TX0_P	MGT	J4B15
M44	MGTFRXN2_131	MGT_131_RX2_N	MGT	J4B16
M43	MGTFRXP2_131	MGT_131_RX2_P	MGT	J4B16
P39	MGTFTXN2_131	MGT_131_TX2_N	MGT	J4B16
P38	MGTFTXP2_131	MGT_131_TX2_P	MGT	J4B16
AY44	MGTFRXN2_124	MGT_124_RX2_N	MGT	J4B2
AY43	MGTFRXP2_124	MGT_124_RX2_P	MGT	J4B2
BD43	MGTFTXN2_124	MGT_124_TX2_N	MGT	J4B2
BD42	MGTFTXP2_124	MGT_124_TX2_P	MGT	J4B2
AV44	MGTFRXN0_125	MGT_125_RX0_N	MGT	J4B3
AV43	MGTFRXP0_125	MGT_125_RX0_P	MGT	J4B3
BB43	MGTFTXN0_125	MGT_125_TX0_N	MGT	J4B3
BB42	MGTFTXP0_125	MGT_125_TX0_P	MGT	J4B3
AT44	MGTFRXN2_125	MGT_125_RX2_N	MGT	J4B4
AT43	MGTFRXP2_125	MGT_125_RX2_P	MGT	J4B4
AW41	MGTFTXN2_125	MGT_125_TX2_N	MGT	J4B4
AW40	MGTFTXP2_125	MGT_125_TX2_P	MGT	J4B4
AP44	MGTFRXN0_126	MGT_126_RX0_N	MGT	J4B5
AP43	MGTFRXP0_126	MGT_126_RX0_P	MGT	J4B5
AT39	MGTFTXN0_126	MGT_126_TX0_N	MGT	J4B5

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
AT38	MGTFTXP0_126	MGT_126_TX0_P	MGT	J4B5
AM44	MGTFRXN2_126	MGT_126_RX2_N	MGT	J4B6
AM43	MGTFRXP2_126	MGT_126_RX2_P	MGT	J4B6
AP39	MGTFTXN2_126	MGT_126_TX2_N	MGT	J4B6
AP38	MGTFTXP2_126	MGT_126_TX2_P	MGT	J4B6
AK44	MGTFRXN0_127	MGT_127_RX0_N	MGT	J4B7
AK43	MGTFRXP0_127	MGT_127_RX0_P	MGT	J4B7
AM39	MGTFTXN0_127	MGT_127_TX0_N	MGT	J4B7
AM38	MGTFTXP0_127	MGT_127_TX0_P	MGT	J4B7
AH44	MGTFRXN2_127	MGT_127_RX2_N	MGT	J4B8
AH43	MGTFRXP2_127	MGT_127_RX2_P	MGT	J4B8
AK39	MGTFTXN2_127	MGT_127_TX2_N	MGT	J4B8
AK38	MGTFTXP2_127	MGT_127_TX2_P	MGT	J4B8
AF44	MGTFRXN0_128	MGT_128_RX0_N	MGT	J4B9
AF43	MGTFRXP0_128	MGT_128_RX0_P	MGT	J4B9
AH39	MGTFTXN0_128	MGT_128_TX0_N	MGT	J4B9
AH38	MGTFTXP0_128	MGT_128_TX0_P	MGT	J4B9
BA46	MGTFRXN1_124	MGT_124_RX1_N	MGT	J4T1
BA45	MGTFRXP1_124	MGT_124_RX1_P	MGT	J4T1
BE41	MGTFTXN1_124	MGT_124_TX1_N	MGT	J4T1
BE40	MGTFTXP1_124	MGT_124_TX1_P	MGT	J4T1
AC46	MGTFRXN3_128	MGT_128_RX3_N	MGT	J4T10
AC45	MGTFRXP3_128	MGT_128_RX3_P	MGT	J4T10
AE41	MGTFTXN3_128	MGT_128_TX3_N	MGT	J4T10
AE40	MGTFTXP3_128	MGT_128_TX3_P	MGT	J4T10
AA46	MGTFRXN1_129	MGT_129_RX1_N	MGT	J4T11
AA45	MGTFRXP1_129	MGT_129_RX1_P	MGT	J4T11
AC41	MGTFTXN1_129	MGT_129_TX1_N	MGT	J4T11
AC40	MGTFTXP1_129	MGT_129_TX1_P	MGT	J4T11
W46	MGTFRXN3_129	MGT_129_RX3_N	MGT	J4T12
W45	MGTFRXP3_129	MGT_129_RX3_P	MGT	J4T12
AA41	MGTFTXN3_129	MGT_129_TX3_N	MGT	J4T12
AA40	MGTFTXP3_129	MGT_129_TX3_P	MGT	J4T12
U46	MGTFRXN1_130	MGT_130_RX1_N	MGT	J4T13
U45	MGTFRXP1_130	MGT_130_RX1_P	MGT	J4T13

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
W41	MGTFTXN1_130	MGT_130_TX1_N	MGT	J4T13
W40	MGTFTXP1_130	MGT_130_TX1_P	MGT	J4T13
R46	MGTFRXN3_130	MGT_130_RX3_N	MGT	J4T14
R45	MGTFRXP3_130	MGT_130_RX3_P	MGT	J4T14
U41	MGTFTXN3_130	MGT_130_TX3_N	MGT	J4T14
U40	MGTFTXP3_130	MGT_130_TX3_P	MGT	J4T14
N46	MGTFRXN1_131	MGT_131_RX1_N	MGT	J4T15
N45	MGTFRXP1_131	MGT_131_RX1_P	MGT	J4T15
R41	MGTFTXN1_131	MGT_131_TX1_N	MGT	J4T15
R40	MGTFTXP1_131	MGT_131_TX1_P	MGT	J4T15
L46	MGTFRXN3_131	MGT_131_RX3_N	MGT	J4T16
L45	MGTFRXP3_131	MGT_131_RX3_P	MGT	J4T16
N41	MGTFTXN3_131	MGT_131_TX3_N	MGT	J4T16
N40	MGTFTXP3_131	MGT_131_TX3_P	MGT	J4T16
AW46	MGTFRXN3_124	MGT_124_RX3_N	MGT	J4T2
AW45	MGTFRXP3_124	MGT_124_RX3_P	MGT	J4T2
BC41	MGTFTXN3_124	MGT_124_TX3_N	MGT	J4T2
BC40	MGTFTXP3_124	MGT_124_TX3_P	MGT	J4T2
AU46	MGTFRXN1_125	MGT_125_RX1_N	MGT	J4T3
AU45	MGTFRXP1_125	MGT_125_RX1_P	MGT	J4T3
BA41	MGTFTXN1_125	MGT_125_TX1_N	MGT	J4T3
BA40	MGTFTXP1_125	MGT_125_TX1_P	MGT	J4T3
AR46	MGTFRXN3_125	MGT_125_RX3_N	MGT	J4T4
AR45	MGTFRXP3_125	MGT_125_RX3_P	MGT	J4T4
AU41	MGTFTXN3_125	MGT_125_TX3_N	MGT	J4T4
AU40	MGTFTXP3_125	MGT_125_TX3_P	MGT	J4T4
AN46	MGTFRXN1_126	MGT_126_RX1_N	MGT	J4T5
AN45	MGTFRXP1_126	MGT_126_RX1_P	MGT	J4T5
AR41	MGTFTXN1_126	MGT_126_TX1_N	MGT	J4T5
AR40	MGTFTXP1_126	MGT_126_TX1_P	MGT	J4T5
AL46	MGTFRXN3_126	MGT_126_RX3_N	MGT	J4T6
AL45	MGTFRXP3_126	MGT_126_RX3_P	MGT	J4T6
AN41	MGTFTXN3_126	MGT_126_TX3_N	MGT	J4T6
AN40	MGTFTXP3_126	MGT_126_TX3_P	MGT	J4T6
AJ46	MGTFRXN1_127	MGT_127_RX1_N	MGT	J4T7

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
AJ45	MGTFRXP1_127	MGT_127_RX1_P	MGT	J4T7
AL41	MGTFTXN1_127	MGT_127_TX1_N	MGT	J4T7
AL40	MGTFTXP1_127	MGT_127_TX1_P	MGT	J4T7
AG46	MGTFRXN3_127	MGT_127_RX3_N	MGT	J4T8
AG45	MGTFRXP3_127	MGT_127_RX3_P	MGT	J4T8
AJ41	MGTFTXN3_127	MGT_127_TX3_N	MGT	J4T8
AJ40	MGTFTXP3_127	MGT_127_TX3_P	MGT	J4T8
AE46	MGTFRXN1_128	MGT_128_RX1_N	MGT	J4T9
AE45	MGTFRXP1_128	MGT_128_RX1_P	MGT	J4T9
AG41	MGTFTXN1_128	MGT_128_TX1_N	MGT	J4T9
AG40	MGTFTXP1_128	MGT_128_TX1_P	MGT	J4T9
H32	IO_L11P_T1U_N8_GC_70	1PPS_1V8	1.8	SMA
E33	IO_L14N_T2L_N3_GC_70	AUX_SCL_FPGA	1.8	-
F33	IO_L14P_T2L_N2_GC_70	AUX_SDA_FPGA	1.8	-
E32	IO_L15N_T2L_N5_AD11N_70	FPGA_SCL_1V8	1.8	-
E31	IO_L15P_T2L_N4_AD11P_70	FPGA_SDA_1V8	1.8	-
E35	IO_L13N_T2L_N1_GC_QBC_70	PRIMARY_CLK_FPGA	1.8	-
F34	IO_L13P_T2L_N0_GC_QBC_70	PRIMARY_DATA_FPGA	1.8	-
G15	IO_L10P_AD10P_93	USER_LED_G0_1V8	1.8	D36
F14	IO_L10N_AD10N_93	USER_LED_G1_1V8	1.8	D37
G14	IO_L11P_AD9P_93	USER_LED_G2_1V8	1.8	D38
F13	IO_L11N_AD9N_93	USER_LED_G3_1V8	1.8	D39
F12	IO_L12P_AD8P_93	USER_LED_G4_1V8	1.8	D40
F11	IO_L12N_AD8N_93	USER_LED_G5_1V8	1.8	D41
K32	IO_T1U_N12_70	AUX_I2C_FPGA_CTRL	1.8	-
L15	IO_L3P_AD13P_93	AVR_B2U_1V8	1.8	-
K16	IO_L5P_HDGC_93	AVR_MON_CLK_1V8	1.8	-
K15	IO_L3N_AD13N_93	AVR_U2B_1V8	1.8	-
AP19	IO_L24N_T3U_N11_DOUT_CSO_B_65	CPRSNT_L	1.8	-
D20	IO_L16N_T2U_N7_QBC_AD3N_72	DDR4_A0	1.2	-
B21	IO_L24P_T3U_N10_72	DDR4_A1	1.2	-
B22	IO_L23P_T3U_N8_72	DDR4_A10	1.2	-
J23	IO_L9N_T1L_N5_AD12N_72	DDR4_A11	1.2	-
F23	IO_L14P_T2L_N2_GC_72	DDR4_A12	1.2	-
J21	IO_L8N_T1L_N3_AD5N_72	DDR4_A13	1.2	-

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
E21	IO_L17P_T2U_N8_AD10P_72	DDR4_A14	1.2	-
E22	IO_L14N_T2L_N3_GC_72	DDR4_A15	1.2	-
A20	IO_L24N_T3U_N11_72	DDR4_A16	1.2	-
A23	IO_L22N_T3U_N7_DBC_AD0N_72	DDR4_A2	1.2	-
D23	IO_T2U_N12_72	DDR4_A3	1.2	-
A24	IO_L22P_T3U_N6_DBC_AD0P_72	DDR4_A4	1.2	-
C22	IO_T3U_N12_72	DDR4_A5	1.2	-
D21	IO_L17N_T2U_N9_AD10N_72	DDR4_A6	1.2	-
E23	IO_L18N_T2U_N11_AD2N_72	DDR4_A7	1.2	-
D24	IO_L20P_T3L_N2_AD1P_72	DDR4_A8	1.2	-
C23	IO_L20N_T3L_N3_AD1N_72	DDR4_A9	1.2	-
C24	IO_L21P_T3L_N4_AD8P_72	DDR4_ACT_N	1.2	-
G24	IO_L10N_T1U_N7_QBC_AD4N_72	DDR4_ALERT_N	1.2	-
E20	IO_L16P_T2U_N6_QBC_AD3P_72	DDR4_BA0	1.2	-
C21	IO_L19P_T3L_N0_DBC_AD9P_72	DDR4_BA1	1.2	-
B24	IO_L21N_T3L_N5_AD8N_72	DDR4_BG0	1.2	-
K22	IO_T1U_N12_72	DDR4_BG1	1.2	-
J20	IO_L7N_T1L_N1_QBC_AD13N_72	DDR4_C0	1.2	-
G20	IO_L15P_T2L_N4_AD11P_72	DDR4_C1	1.2	-
G21	IO_L12N_T1U_N11_GC_72	DDR4_CK0_C	1.2	-
H21	IO_L12P_T1U_N10_GC_72	DDR4_CK0_T	1.2	-
F22	IO_L13N_T2L_N1_GC_QBC_72	DDR4_CK1_C	1.2	-
G22	IO_L13P_T2L_N0_GC_QBC_72	DDR4_CK1_T	1.2	-
H24	IO_L10P_T1U_N6_QBC_AD4P_72	DDR4_CKE0	1.2	-
J24	IO_L9P_T1L_N4_AD12P_72	DDR4_CKE1	1.2	-
B20	IO_L19N_T3L_N1_DBC_AD9N_72	DDR4_CS0	1.2	-
K21	IO_L8P_T1L_N2_AD5P_72	DDR4_CS1	1.2	-
C28	IO_L19P_T3L_N0_DBC_AD9P_71	DDR4_DM0	1.2	-
N26	IO_L1P_T0L_N0_DBC_71	DDR4_DM1	1.2	-
F27	IO_L13P_T2L_N0_GC_QBC_71	DDR4_DM2	1.2	-
J28	IO_L7P_T1L_N0_QBC_AD13P_71	DDR4_DM3	1.2	-
E13	IO_L19P_T3L_N0_DBC_AD9P_73	DDR4_DM4	1.2	-
G19	IO_L7P_T1L_N0_QBC_AD13P_73	DDR4_DM5	1.2	-
M17	IO_L1P_T0L_N0_DBC_73	DDR4_DM6	1.2	-
C17	IO_L13P_T2L_N0_GC_QBC_73	DDR4_DM7	1.2	-

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
N24	IO_L1P_T0L_N0_DBC_72	DDR4_DM8	1.2	-
B29	IO_L21P_T3L_N4_AD8P_71	DDR4_DQ0	1.2	-
A29	IO_L21N_T3L_N5_AD8N_71	DDR4_DQ1	1.2	-
K25	IO_L6P_T0U_N10_AD6P_71	DDR4_DQ10	1.2	-
L25	IO_L5P_T0U_N8_AD14P_71	DDR4_DQ11	1.2	-
M27	IO_L2N_T0L_N3_71	DDR4_DQ12	1.2	-
L28	IO_L3P_T0L_N4_AD15P_71	DDR4_DQ13	1.2	-
N27	IO_L2P_T0L_N2_71	DDR4_DQ14	1.2	-
J25	IO_L6N_T0U_N11_AD6N_71	DDR4_DQ15	1.2	-
C26	IO_L18N_T2U_N11_AD2N_71	DDR4_DQ16	1.2	-
D26	IO_L18P_T2U_N10_AD2P_71	DDR4_DQ17	1.2	-
E27	IO_L14N_T2L_N3_GC_71	DDR4_DQ18	1.2	-
E26	IO_L14P_T2L_N2_GC_71	DDR4_DQ19	1.2	-
A25	IO_L24N_T3U_N11_71	DDR4_DQ2	1.2	-
E30	IO_L15P_T2L_N4_AD11P_71	DDR4_DQ20	1.2	-
D30	IO_L15N_T2L_N5_AD11N_71	DDR4_DQ21	1.2	-
E25	IO_L17P_T2U_N8_AD10P_71	DDR4_DQ22	1.2	-
D25	IO_L17N_T2U_N9_AD10N_71	DDR4_DQ23	1.2	-
G29	IO_L9P_T1L_N4_AD12P_71	DDR4_DQ24	1.2	-
G26	IO_L12P_T1U_N10_GC_71	DDR4_DQ25	1.2	-
H27	IO_L11N_T1U_N9_GC_71	DDR4_DQ26	1.2	-
J29	IO_L8P_T1L_N2_AD5P_71	DDR4_DQ27	1.2	-
F29	IO_L9N_T1L_N5_AD12N_71	DDR4_DQ28	1.2	-
G27	IO_L12N_T1U_N11_GC_71	DDR4_DQ29	1.2	-
B26	IO_L23P_T3U_N8_71	DDR4_DQ3	1.2	-
H26	IO_L11P_T1U_N8_GC_71	DDR4_DQ30	1.2	-
H29	IO_L8N_T1L_N3_AD5N_71	DDR4_DQ31	1.2	-
A13	IO_L21P_T3L_N4_AD8P_73	DDR4_DQ32	1.2	-
A12	IO_L21N_T3L_N5_AD8N_73	DDR4_DQ33	1.2	-
E12	IO_L24P_T3U_N10_73	DDR4_DQ34	1.2	-
E11	IO_L24N_T3U_N11_73	DDR4_DQ35	1.2	-
C13	IO_L20P_T3L_N2_AD1P_73	DDR4_DQ36	1.2	-
C12	IO_L20N_T3L_N3_AD1N_73	DDR4_DQ37	1.2	-
C11	IO_L23N_T3U_N9_73	DDR4_DQ38	1.2	-
D11	IO_L23P_T3U_N8_73	DDR4_DQ39	1.2	-

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
B30	IO_L20P_T3L_N2_AD1P_71	DDR4_DQ4	1.2	-
B19	IO_L9P_T1L_N4_AD12P_73	DDR4_DQ40	1.2	-
C19	IO_L8N_T1L_N3_AD5N_73	DDR4_DQ41	1.2	-
E17	IO_L11N_T1U_N9_GC_73	DDR4_DQ42	1.2	-
E18	IO_L11P_T1U_N8_GC_73	DDR4_DQ43	1.2	-
A19	IO_L9N_T1L_N5_AD12N_73	DDR4_DQ44	1.2	-
D19	IO_L8P_T1L_N2_AD5P_73	DDR4_DQ45	1.2	-
C18	IO_L12N_T1U_N11_GC_73	DDR4_DQ46	1.2	-
D18	IO_L12P_T1U_N10_GC_73	DDR4_DQ47	1.2	-
L18	IO_L2P_T0L_N2_73	DDR4_DQ48	1.2	-
J18	IO_L5P_T0U_N8_AD14P_73	DDR4_DQ49	1.2	-
A30	IO_L20N_T3L_N3_AD1N_71	DDR4_DQ5	1.2	-
H17	IO_L5N_T0U_N9_AD14N_73	DDR4_DQ50	1.2	-
F17	IO_L6N_T0U_N11_AD6N_73	DDR4_DQ51	1.2	-
K18	IO_L3N_T0L_N5_AD15N_73	DDR4_DQ52	1.2	-
L19	IO_L3P_T0L_N4_AD15P_73	DDR4_DQ53	1.2	-
G17	IO_L6P_T0U_N10_AD6P_73	DDR4_DQ54	1.2	-
K17	IO_L2N_T0L_N3_73	DDR4_DQ55	1.2	-
A15	IO_L15P_T2L_N4_AD11P_73	DDR4_DQ56	1.2	-
B16	IO_L14N_T2L_N3_GC_73	DDR4_DQ57	1.2	-
D14	IO_L17N_T2U_N9_AD10N_73	DDR4_DQ58	1.2	-
E15	IO_L18N_T2U_N11_AD2N_73	DDR4_DQ59	1.2	-
B25	IO_L24P_T3U_N10_71	DDR4_DQ6	1.2	-
B17	IO_L14P_T2L_N2_GC_73	DDR4_DQ60	1.2	-
A14	IO_L15N_T2L_N5_AD11N_73	DDR4_DQ61	1.2	-
D15	IO_L17P_T2U_N8_AD10P_73	DDR4_DQ62	1.2	-
E16	IO_L18P_T2U_N10_AD2P_73	DDR4_DQ63	1.2	-
L24	IO_L2N_T0L_N3_72	DDR4_DQ64	1.2	-
K23	IO_L3N_T0L_N5_AD15N_72	DDR4_DQ65	1.2	-
M21	IO_L5N_T0U_N9_AD14N_72	DDR4_DQ66	1.2	-
M20	IO_L6P_T0U_N10_AD6P_72	DDR4_DQ67	1.2	-
M24	IO_L2P_T0L_N2_72	DDR4_DQ68	1.2	-
L23	IO_L3P_T0L_N4_AD15P_72	DDR4_DQ69	1.2	-
A27	IO_L23N_T3U_N9_71	DDR4_DQ7	1.2	-
L20	IO_L6N_T0U_N11_AD6N_72	DDR4_DQ70	1.2	-

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
N21	IO_L5P_T0U_N8_AD14P_72	DDR4_DQ71	1.2	-
L29	IO_L3N_T0L_N5_AD15N_71	DDR4_DQ8	1.2	-
K26	IO_L5N_T0U_N9_AD14N_71	DDR4_DQ9	1.2	-
A28	IO_L22N_T3U_N7_DBC_AD0N_71	DDR4_DQS0_C	1.2	-
B27	IO_L22P_T3U_N6_DBC_AD0P_71	DDR4_DQS0_T	1.2	-
K28	IO_L4N_T0U_N7_DBC_AD7N_71	DDR4_DQS1_C	1.2	-
K27	IO_L4P_T0U_N6_DBC_AD7P_71	DDR4_DQS1_T	1.2	-
D29	IO_L16N_T2U_N7_QBC_AD3N_71	DDR4_DQS2_C	1.2	-
E28	IO_L16P_T2U_N6_QBC_AD3P_71	DDR4_DQS2_T	1.2	-
F25	IO_L10N_T1U_N7_QBC_AD4N_71	DDR4_DQS3_C	1.2	-
G25	IO_L10P_T1U_N6_QBC_AD4P_71	DDR4_DQS3_T	1.2	-
B11	IO_L22N_T3U_N7_DBC_AD0N_73	DDR4_DQS4_C	1.2	-
B12	IO_L22P_T3U_N6_DBC_AD0P_73	DDR4_DQS4_T	1.2	-
A17	IO_L10N_T1U_N7_QBC_AD4N_73	DDR4_DQS5_C	1.2	-
A18	IO_L10P_T1U_N6_QBC_AD4P_73	DDR4_DQS5_T	1.2	-
H19	IO_L4N_T0U_N7_DBC_AD7N_73	DDR4_DQS6_C	1.2	-
J19	IO_L4P_T0U_N6_DBC_AD7P_73	DDR4_DQS6_T	1.2	-
B14	IO_L16N_T2U_N7_QBC_AD3N_73	DDR4_DQS7_C	1.2	-
B15	IO_L16P_T2U_N6_QBC_AD3P_73	DDR4_DQS7_T	1.2	-
M22	IO_L4N_T0U_N7_DBC_AD7N_72	DDR4_DQS8_C	1.2	-
N22	IO_L4P_T0U_N6_DBC_AD7P_72	DDR4_DQS8_T	1.2	-
F20	IO_L15N_T2L_N5_AD11N_72	DDR4_ODT0	1.2	-
K20	IO_L7P_T1L_N0_QBC_AD13P_72	DDR4_ODT1	1.2	-
A22	IO_L23N_T3U_N9_72	DDR4_PAR	1.2	-
F24	IO_L18P_T2U_N10_AD2P_72	DDR4_RESET_N	1.2	-
L30	IO_L3N_T0L_N5_AD15N_70	FIREFLY_0_MODSEL_L	1.8	-
K30	IO_L4P_T0U_N6_DBC_AD7P_70	FIREFLY_1_MODSEL_L	1.8	-
J30	IO_L4N_T0U_N7_DBC_AD7N_70	FIREFLY_2_MODSEL_L	1.8	-
K31	IO_L5P_T0U_N8_AD14P_70	FIREFLY_3_MODSEL_L	1.8	-
J31	IO_L5N_T0U_N9_AD14N_70	FIREFLY_4_MODSEL_L	1.8	-
K33	IO_L6P_T0U_N10_AD6P_70	FIREFLY_5_MODSEL_L	1.8	-
J33	IO_L6N_T0U_N11_AD6N_70	FIREFLY_6_MODSEL_L	1.8	-
L32	IO_T0U_N12_VRP_70	FIREFLY_7_MODSEL_L	1.8	-
J34	IO_L7P_T1L_N0_QBC_AD13P_70	FIREFLY_8_MODSEL_L	1.8	-
H34	IO_L7N_T1L_N1_QBC_AD13N_70	FIREFLY_9_MODSEL_L	1.8	-

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
H8	MGTREFCLK0N_232	FIREFLY_CLK_0_PIN_N	MGT REFCLK	-
H9	MGTREFCLK0P_232	FIREFLY_CLK_0_PIN_P	MGT REFCLK	-
AA10	MGTREFCLK0N_229	FIREFLY_CLK_1_PIN_N	MGT REFCLK	-
AA11	MGTREFCLK0P_229	FIREFLY_CLK_1_PIN_P	MGT REFCLK	-
AG10	MGTREFCLK1N_227	FIREFLY_CLK_2_PIN_N	MGT REFCLK	-
AG11	MGTREFCLK1P_227	FIREFLY_CLK_2_PIN_P	MGT REFCLK	-
D39	MGTREFCLK0N_133	FIREFLY_CLK_3_PIN_N	MGT REFCLK	-
D38	MGTREFCLK0P_133	FIREFLY_CLK_3_PIN_P	MGT REFCLK	-
F35	IO_L8N_T1L_N3_AD5N_70	FIREFLY_INTL_1V8_L	1.8	-
H31	IO_L9P_T1L_N4_AD12P_70	FIREFLY_RESET_1V8_L	1.8	-
G30	IO_L10P_T1U_N6_QBC_AD4P_70	FIREFLY_SCL_1V8	1.8	-
G31	IO_L9N_T1L_N5_AD12N_70	FIREFLY_SDA_1V8	1.8	-
BC11	RDWR_FCS_B_0	FPGA_FLASH_CE0_L	1.8	-
BD13	D00_MOSI_0	FPGA_FLASH_DQ0	1.8	-
BE12	D01_DIN_0	FPGA_FLASH_DQ1	1.8	-
BD11	D02_0	FPGA_FLASH_DQ2	1.8	-
BE11	D03_0	FPGA_FLASH_DQ3	1.8	-
R37	MGTREFCLK0N_130	MEZ_CLK_0_PIN_N	MGT REFCLK	-
R36	MGTREFCLK0P_130	MEZ_CLK_0_PIN_P	MGT REFCLK	-
AC37	MGTREFCLK0N_128	MEZ_CLK_1_PIN_N	MGT REFCLK	-
AC36	MGTREFCLK0P_128	MEZ_CLK_1_PIN_P	MGT REFCLK	-
AG37	MGTREFCLK0N_127	MEZ_CLK_2_PIN_N	MGT REFCLK	-
AG36	MGTREFCLK0P_127	MEZ_CLK_2_PIN_P	MGT REFCLK	-
AU37	MGTREFCLK0N_125	MEZ_CLK_3_PIN_N	MGT REFCLK	-
AU36	MGTREFCLK0P_125	MEZ_CLK_3_PIN_P	MGT REFCLK	-
AR10	MGTREFCLK1N_225	PCIE_LCL_REFCLK_PIN_N	MGT REFCLK	-
AR11	MGTREFCLK1P_225	PCIE_LCL_REFCLK_PIN_P	MGT REFCLK	-
AV8	MGTREFCLK0N_225	PCIE_REFCLKA_PIN_N	MGT REFCLK	-
AV9	MGTREFCLK0P_225	PCIE_REFCLKA_PIN_P	MGT REFCLK	-
BB8	MGTREFCLK0N_224	PCIE_REFCLKB_PIN_N	MGT REFCLK	-
BB9	MGTREFCLK0P_224	PCIE_REFCLKB_PIN_P	MGT REFCLK	-
AT3	MGTYRXN3_225	PCIE_RX0_N	MGT	-
AT4	MGTYRXP3_225	PCIE_RX0_P	MGT	-
AU1	MGTYRXN2_225	PCIE_RX1_N	MGT	-
AU2	MGTYRXP2_225	PCIE_RX1_P	MGT	-

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
AV3	MGTYRXN1_225	PCIE_RX2_N	MGT	-
AV4	MGTYRXP1_225	PCIE_RX2_P	MGT	-
AW1	MGTYRXN0_225	PCIE_RX3_N	MGT	-
AW2	MGTYRXP0_225	PCIE_RX3_P	MGT	-
AY3	MGTYRXN3_224	PCIE_RX4_N	MGT	-
AY4	MGTYRXP3_224	PCIE_RX4_P	MGT	-
BA1	MGTYRXN2_224	PCIE_RX5_N	MGT	-
BA2	MGTYRXP2_224	PCIE_RX5_P	MGT	-
BB3	MGTYRXN1_224	PCIE_RX6_N	MGT	-
BB4	MGTYRXP1_224	PCIE_RX6_P	MGT	-
BC1	MGTYRXN0_224	PCIE_RX7_N	MGT	-
BC2	MGTYRXP0_224	PCIE_RX7_P	MGT	-
AW6	MGTYTXN3_225	PCIE_TX0_PIN_N	MGT	-
AW7	MGTYTXP3_225	PCIE_TX0_PIN_P	MGT	-
BA6	MGTYTXN2_225	PCIE_TX1_PIN_N	MGT	-
BA7	MGTYTXP2_225	PCIE_TX1_PIN_P	MGT	-
BC6	MGTYTXN1_225	PCIE_TX2_PIN_N	MGT	-
BC7	MGTYTXP1_225	PCIE_TX2_PIN_P	MGT	-
BD8	MGTYTXN0_225	PCIE_TX3_PIN_N	MGT	-
BD9	MGTYTXP0_225	PCIE_TX3_PIN_P	MGT	-
BD4	MGTYTXN3_224	PCIE_TX4_PIN_N	MGT	-
BD5	MGTYTXP3_224	PCIE_TX4_PIN_P	MGT	-
BE6	MGTYTXN2_224	PCIE_TX5_PIN_N	MGT	-
BE7	MGTYTXP2_224	PCIE_TX5_PIN_P	MGT	-
BF8	MGTYTXN1_224	PCIE_TX6_PIN_N	MGT	-
BF9	MGTYTXP1_224	PCIE_TX6_PIN_P	MGT	-
BF4	MGTYTXN0_224	PCIE_TX7_PIN_N	MGT	-
BF5	MGTYTXP0_224	PCIE_TX7_PIN_P	MGT	-
AT19	IO_T3U_N12_PERSTN0_65	PERST0_1V5_L	1.5	-
C31	IO_L16N_T2U_N7_QBC_AD3N_70	PRIMARY_I2C_FPGA_CTRL	1.8	-
BE22	IO_L4N_T0U_N7_DBC_AD7N_66	QDR2_0_A0	1.5	-
BA22	IO_T1U_N12_66	QDR2_0_A1	1.5	-
BF23	IO_L2P_T0L_N2_66	QDR2_0_A10	1.5	-
BA25	IO_L7P_T1L_N0_QBC_AD13P_66	QDR2_0_A11	1.5	-
BF25	IO_L1P_T0L_N0_DBC_66	QDR2_0_A12	1.5	-

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
BE25	IO_L5N_T0U_N9_AD14N_66	QDR2_0_A13	1.5	-
BE23	IO_L4P_T0U_N6_DBC_AD7P_66	QDR2_0_A14	1.5	-
AU25	IO_L16P_T2U_N6_QBC_AD3P_66	QDR2_0_A15	1.5	-
AU24	IO_L16N_T2U_N7_QBC_AD3N_66	QDR2_0_A16	1.5	-
BA24	IO_L12P_T1U_N10_GC_66	QDR2_0_A17	1.5	-
BB25	IO_L7N_T1L_N1_QBC_AD13N_66	QDR2_0_A18	1.5	-
BB24	IO_L8P_T1L_N2_AD5P_66	QDR2_0_A19	1.5	-
BB21	IO_L9P_T1L_N4_AD12P_66	QDR2_0_A2	1.5	-
BD23	IO_L6N_T0U_N11_AD6N_66	QDR2_0_A20_144	1.5	-
AW21	IO_L10P_T1U_N6_QBC_AD4P_66	QDR2_0_A21_288	1.5	-
BD21	IO_L3P_T0L_N4_AD15P_66	QDR2_0_A22_NC	1.5	-
BE21	IO_L3N_T0L_N5_AD15N_66	QDR2_0_A3	1.5	-
BB22	IO_L11P_T1U_N8_GC_66	QDR2_0_A4	1.5	-
BA23	IO_L12N_T1U_N11_GC_66	QDR2_0_A5	1.5	-
BC21	IO_L9N_T1L_N5_AD12N_66	QDR2_0_A6	1.5	-
BC23	IO_L6P_T0U_N10_AD6P_66	QDR2_0_A7	1.5	-
BF24	IO_L1N_T0L_N1_DBC_66	QDR2_0_A8	1.5	-
BC24	IO_L8N_T1L_N3_AD5N_66	QDR2_0_A9	1.5	-
AR16	IO_L19N_T3L_N1_DBC_AD9N_D11_65	QDR2_0_BWS0_N	1.5	-
BA18	IO_L13N_T2L_N1_GC_QBC_A07-_D23_65	QDR2_0_BWS1_N	1.5	-
BA20	IO_L7P_T1L_N0_QBC_AD13P_A18_65	QDR2_0_CQ	1.5	-
AW16	IO_L10P_T1U_N6_QBC_AD4P_A-12_D28_65	"QDR2_0_CQ""#"""	1.5	-
AP18	IO_L20P_T3L_N2_AD1P_D08_65	QDR2_0_D0	1.5	-
AR20	IO_L23P_T3U_N8_I2C_SCLK_65	QDR2_0_D1	1.5	-
AU16	IO_L18N_T2U_N11_AD2N_D13_65	QDR2_0_D10	1.5	-
AV17	IO_L16N_T2U_N7_QBC_AD3N_A-01_D17_65	QDR2_0_D11	1.5	-
AU17	IO_L17P_T2U_N8_AD10P_D14_65	QDR2_0_D12	1.5	-
AY18	IO_L13P_T2L_N0_GC_QBC_A06_-D22_65	QDR2_0_D13	1.5	-
AV18	IO_L16P_T2U_N6_QBC_AD3P_A-00_D16_65	QDR2_0_D14	1.5	-
AW20	IO_L15P_T2L_N4_AD11P_A02_D18_65	QDR2_0_D15	1.5	-
AY20	IO_L15N_T2L_N5_AD11N_A03_D19_65	QDR2_0_D16	1.5	-

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
AT17	IO_L18P_T2U_N10_AD2P_D12_65	QDR2_0_D17	1.5	-
AT20	IO_L23N_T3U_N9_PERSTN1_I2C-_SDA_65	QDR2_0_D2	1.5	-
AU20	IO_L22P_T3U_N6_DBC_AD0P_D04_65	QDR2_0_D3	1.5	-
AU19	IO_L22N_T3U_N7_DBC_AD0N_D05_65	QDR2_0_D4	1.5	-
AT18	IO_L21N_T3L_N5_AD8N_D07_65	QDR2_0_D5	1.5	-
AR18	IO_L21P_T3L_N4_AD8P_D06_65	QDR2_0_D6	1.5	-
AR17	IO_L20N_T3L_N3_AD1N_D09_65	QDR2_0_D7	1.5	-
AP16	IO_L19P_T3L_N0_DBC_AD9P_D10_65	QDR2_0_D8	1.5	-
AV16	IO_L17N_T2U_N9_AD10N_D15_65	QDR2_0_D9	1.5	-
BF22	IO_L2N_T0L_N3_66	QDR2_0_DOFF_N	1.5	-
AW18	IO_L14N_T2L_N3_GC_A05_D21_65	QDR2_0_K_N	1.5	-
AW19	IO_L14P_T2L_N2_GC_A04_D20_65	QDR2_0_K_P	1.5	-
AY25	IO_L15N_T2L_N5_AD11N_66	QDR2_0_ODT	1.5	-
BB20	IO_L7N_T1L_N1_QBC_AD13N_A19_65	QDR2_0_Q0	1.5	-
BF20	IO_L4P_T0U_N6_DBC_AD7P_A24_65	QDR2_0_Q1	1.5	-
BD16	IO_L1P_T0L_N0_DBC_RS0_65	QDR2_0_Q10	1.5	-
BC17	IO_L8N_T1L_N3_AD5N_A17_65	QDR2_0_Q11	1.5	-
BE18	IO_L3P_T0L_N4_AD15P_A26_65	QDR2_0_Q12	1.5	-
BF18	IO_L3N_T0L_N5_AD15N_A27_65	QDR2_0_Q13	1.5	-
BD19	IO_L6N_T0U_N11_AD6N_A21_65	QDR2_0_Q14	1.5	-
BB19	IO_L11N_T1U_N9_GC_A11_D27_65	QDR2_0_Q15	1.5	-
BD20	IO_L5P_T0U_N8_AD14P_A22_65	QDR2_0_Q16	1.5	-
BA19	IO_L11P_T1U_N8_GC_A10_D26_65	QDR2_0_Q17	1.5	-
BE20	IO_L5N_T0U_N9_AD14N_A23_65	QDR2_0_Q2	1.5	-
BF19	IO_L4N_T0U_N7_DBC_AD7N_A25_65	QDR2_0_Q3	1.5	-
BC19	IO_L6P_T0U_N10_AD6P_A20_65	QDR2_0_Q4	1.5	-
BE17	IO_L2P_T0L_N2_FOE_B_65	QDR2_0_Q5	1.5	-
BB17	IO_L8P_T1L_N2_AD5P_A16_65	QDR2_0_Q6	1.5	-
BC16	IO_L9N_T1L_N5_AD12N_A15_D31_65	QDR2_0_Q7	1.5	-
AY16	IO_L10N_T1U_N7_QBC_AD4N_A-13_D29_65	QDR2_0_Q8	1.5	-
BB16	IO_L9P_T1L_N4_AD12P_A14_D30_65	QDR2_0_Q9	1.5	-
AY21	IO_L10N_T1U_N7_QBC_AD4N_66	QDR2_0_RPS_N	1.5	-
BC22	IO_L11N_T1U_N9_GC_66	QDR2_0_WPS_N	1.5	-

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
BC28	IO_T1U_N12_67	QDR2_1_A0	1.5	-
AU31	IO_L21N_T3L_N5_AD8N_67	QDR2_1_A1	1.5	-
AY27	IO_T2U_N12_67	QDR2_1_A10	1.5	-
AT29	IO_L22P_T3U_N6_DBC_AD0P_67	QDR2_1_A11	1.5	-
AW28	IO_L17N_T2U_N9_AD10N_67	QDR2_1_A12	1.5	-
AV28	IO_L17P_T2U_N8_AD10P_67	QDR2_1_A13	1.5	-
AU26	IO_L19P_T3L_N0_DBC_AD9P_67	QDR2_1_A14	1.5	-
AR28	IO_L23P_T3U_N8_67	QDR2_1_A15	1.5	-
AR27	IO_L24P_T3U_N10_67	QDR2_1_A16	1.5	-
AT28	IO_L23N_T3U_N9_67	QDR2_1_A17	1.5	-
AU29	IO_T3U_N12_67	QDR2_1_A18	1.5	-
AT27	IO_L24N_T3U_N11_67	QDR2_1_A19	1.5	-
AU30	IO_L22N_T3U_N7_DBC_AD0N_67	QDR2_1_A2	1.5	-
AW26	IO_L18P_T2U_N10_AD2P_67	QDR2_1_A20_144	1.5	-
AV31	IO_L15P_T2L_N4_AD11P_67	QDR2_1_A21_288	1.5	-
AY26	IO_L18N_T2U_N11_AD2N_67	QDR2_1_A22_NC	1.5	-
AW29	IO_L16N_T2U_N7_QBC_AD3N_67	QDR2_1_A3	1.5	-
AY31	IO_L14N_T2L_N3_GC_67	QDR2_1_A4	1.5	-
BA29	IO_L13N_T2L_N1_GC_QBC_67	QDR2_1_A5	1.5	-
AW31	IO_L15N_T2L_N5_AD11N_67	QDR2_1_A6	1.5	-
AV27	IO_L20N_T3L_N3_AD1N_67	QDR2_1_A7	1.5	-
AY28	IO_L13P_T2L_N0_GC_QBC_67	QDR2_1_A8	1.5	-
AU27	IO_L20P_T3L_N2_AD1P_67	QDR2_1_A9	1.5	-
BB37	IO_L10P_T1U_N6_QBC_AD4P_68	QDR2_1_BWS0_N	1.5	-
BE32	IO_L3P_T0L_N4_AD15P_68	QDR2_1_BWS1_N	1.5	-
AY32	IO_L16P_T2U_N6_QBC_AD3P_68	QDR2_1_CQ	1.5	-
BA35	IO_L13P_T2L_N0_GC_QBC_68	"QDR2_1_CQ""#"""	1.5	-
BC37	IO_L10N_T1U_N7_QBC_AD4N_68	QDR2_1_D0	1.5	-
BC36	IO_L12P_T1U_N10_GC_68	QDR2_1_D1	1.5	-
BD31	IO_L4P_T0U_N6_DBC_AD7P_68	QDR2_1_D10	1.5	-
BF32	IO_L3N_T0L_N5_AD15N_68	QDR2_1_D11	1.5	-
BF33	IO_L2P_T0L_N2_68	QDR2_1_D12	1.5	-
BF34	IO_L2N_T0L_N3_68	QDR2_1_D13	1.5	-
BF35	IO_L1N_T0L_N1_DBC_68	QDR2_1_D14	1.5	-
BE35	IO_L1P_T0L_N0_DBC_68	QDR2_1_D15	1.5	-

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
BC32	IO_L5P_T0U_N8_AD14P_68	QDR2_1_D16	1.5	-
BD33	IO_L5N_T0U_N9_AD14N_68	QDR2_1_D17	1.5	-
BF38	IO_L8N_T1L_N3_AD5N_68	QDR2_1_D2	1.5	-
BE38	IO_L8P_T1L_N2_AD5P_68	QDR2_1_D3	1.5	-
BF37	IO_L7N_T1L_N1_QBC_AD13N_68	QDR2_1_D4	1.5	-
BE37	IO_L7P_T1L_N0_QBC_AD13P_68	QDR2_1_D5	1.5	-
BD36	IO_L12N_T1U_N11_GC_68	QDR2_1_D6	1.5	-
BD35	IO_L11N_T1U_N9_GC_68	QDR2_1_D7	1.5	-
BC34	IO_L11P_T1U_N8_GC_68	QDR2_1_D8	1.5	-
BE31	IO_L4N_T0U_N7_DBC_AD7N_68	QDR2_1_D9	1.5	-
AV26	IO_L19N_T3L_N1_DBC_AD9N_67	QDR2_1_DOFF_N	1.5	-
BD38	IO_L9N_T1L_N5_AD12N_68	QDR2_1_K_N	1.5	-
BC38	IO_L9P_T1L_N4_AD12P_68	QDR2_1_K_P	1.5	-
AT30	IO_L21P_T3L_N4_AD8P_67	QDR2_1_ODT	1.5	-
AW36	IO_L18P_T2U_N10_AD2P_68	QDR2_1_Q0	1.5	-
AW35	IO_L17P_T2U_N8_AD10P_68	QDR2_1_Q1	1.5	-
AV32	IO_L21N_T3L_N5_AD8N_68	QDR2_1_Q10	1.5	-
AW33	IO_L19P_T3L_N0_DBC_AD9P_68	QDR2_1_Q11	1.5	-
AV33	IO_L20P_T3L_N2_AD1P_68	QDR2_1_Q12	1.5	-
BB34	IO_L14P_T2L_N2_GC_68	QDR2_1_Q13	1.5	-
BB35	IO_L14N_T2L_N3_GC_68	QDR2_1_Q14	1.5	-
BB36	IO_L13N_T2L_N1_GC_QBC_68	QDR2_1_Q15	1.5	-
AW34	IO_L20N_T3L_N3_AD1N_68	QDR2_1_Q16	1.5	-
AU34	IO_L22P_T3U_N6_DBC_AD0P_68	QDR2_1_Q17	1.5	-
AY36	IO_L18N_T2U_N11_AD2N_68	QDR2_1_Q2	1.5	-
AY35	IO_L17N_T2U_N9_AD10N_68	QDR2_1_Q3	1.5	-
BA34	IO_T2U_N12_68	QDR2_1_Q4	1.5	-
BA33	IO_L16N_T2U_N7_QBC_AD3N_68	QDR2_1_Q5	1.5	-
AY33	IO_L19N_T3L_N1_DBC_AD9N_68	QDR2_1_Q6	1.5	-
BB32	IO_L15N_T2L_N5_AD11N_68	QDR2_1_Q7	1.5	-
BA32	IO_L15P_T2L_N4_AD11P_68	QDR2_1_Q8	1.5	-
AU32	IO_L21P_T3L_N4_AD8P_68	QDR2_1_Q9	1.5	-
AW30	IO_L14P_T2L_N2_GC_67	QDR2_1_RPS_N	1.5	-
AV29	IO_L16P_T2U_N6_QBC_AD3P_67	QDR2_1_WPS_N	1.5	-
F32	IO_L12N_T1U_N11_GC_70	REFCLK200_0_PIN_N	1.8	-

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
G32	IO_L12P_T1U_N10_GC_70	REFCLK200_0_PIN_P	1.8	-
AY22	IO_L13N_T2L_N1_GC_QBC_66	REFCLK200_1_PIN_N	1.8	-
AW23	IO_L13P_T2L_N0_GC_QBC_66	REFCLK200_1_PIN_P	1.8	-
BC27	IO_L11N_T1U_N9_GC_67	REFCLK200_2_PIN_N	1.8	-
BB27	IO_L11P_T1U_N8_GC_67	REFCLK200_2_PIN_P	1.8	-
H22	IO_L11N_T1U_N9_GC_72	REFCLK200_3_PIN_N	1.8	-
H23	IO_L11P_T1U_N8_GC_72	REFCLK200_3_PIN_P	1.8	-
AY15	IO_L6N_HDGC_AD6N_88	SI5328_0_CLKIN1_N	1.8	-
AW15	IO_L6P_HDGC_AD6P_88	SI5328_0_CLKIN1_P	1.8	-
AA37	MGTREFCLK1N_128	SI5328_0_CLKIN2_N	MGT REFCLK	-
AA36	MGTREFCLK1P_128	SI5328_0_CLKIN2_P	MGT REFCLK	-
L37	MGTREFCLK0N_131	SI5328_0_CLKOUT1_PIN_N	MGT REFCLK	-
L36	MGTREFCLK0P_131	SI5328_0_CLKOUT1_PIN_P	MGT REFCLK	-
W37	MGTREFCLK0N_129	SI5328_0_CLKOUT2_PIN_N	MGT REFCLK	-
W36	MGTREFCLK0P_129	SI5328_0_CLKOUT2_PIN_P	MGT REFCLK	-
BF15	IO_L1P_AD11P_88	SI5328_0_INT_C1B	1.8	-
BF14	IO_L1N_AD11N_88	SI5328_0_LOL	1.8	-
AR15	IO_L10P_AD2P_88	SI5328_0_RST_L	1.8	-
AW14	IO_L7N_HDGC_AD5N_88	SI5328_1_CLKIN1_N	1.8	-
AV14	IO_L7P_HDGC_AD5P_88	SI5328_1_CLKIN1_P	1.8	-
AE37	MGTREFCLK1N_127	SI5328_1_CLKIN2_N	MGT REFCLK	-
AE36	MGTREFCLK1P_127	SI5328_1_CLKIN2_P	MGT REFCLK	-
AL37	MGTREFCLK0N_126	SI5328_1_CLKOUT1_PIN_N	MGT REFCLK	-
AL36	MGTREFCLK0P_126	SI5328_1_CLKOUT1_PIN_P	MGT REFCLK	-
AY39	MGTREFCLK0N_124	SI5328_1_CLKOUT2_PIN_N	MGT REFCLK	-
AY38	MGTREFCLK0P_124	SI5328_1_CLKOUT2_PIN_P	MGT REFCLK	-
BD15	IO_L2P_AD10P_88	SI5328_1_INT_C1B	1.8	-
BE15	IO_L2N_AD10N_88	SI5328_1_LOL	1.8	-
AT15	IO_L10N_AD2N_88	SI5328_1_RST_L	1.8	-
BB15	IO_L5N_HDGC_AD7N_88	SI5328_2_CLKIN1_N	1.8	-
BA15	IO_L5P_HDGC_AD7P_88	SI5328_2_CLKIN1_P	1.8	-
W10	MGTREFCLK1N_229	SI5328_2_CLKIN2_N	MGT REFCLK	-
W11	MGTREFCLK1P_229	SI5328_2_CLKIN2_P	MGT REFCLK	-
D8	MGTREFCLK0N_233	SI5328_2_CLKOUT1_PIN_N	MGT REFCLK	-
D9	MGTREFCLK0P_233	SI5328_2_CLKOUT1_PIN_P	MGT REFCLK	-

Table 11 : AD01474 pinout (continued on next page)

FPGA Pin	FPGA Pin Name	Signal Name	IO Voltage	Front Panel Ref
U10	MGTREFCLK0N_230	SI5328_2_CLKOUT2_PIN_N	MGT REFCLK	-
U11	MGTREFCLK0P_230	SI5328_2_CLKOUT2_PIN_P	MGT REFCLK	-
BC14	IO_L3P_AD9P_88	SI5328_2_INT_C1B	1.8	-
BD14	IO_L3N_AD9N_88	SI5328_2_LOL	1.8	-
AP15	IO_L11P_AD1P_88	SI5328_2_RST_L	1.8	-
AU14	IO_L8N_HDGC_AD4N_88	SI5328_3_CLKIN1_N	1.8	-
AU15	IO_L8P_HDGC_AD4P_88	SI5328_3_CLKIN1_P	1.8	-
AL10	MGTREFCLK1N_226	SI5328_3_CLKIN2_N	MGT REFCLK	-
AL11	MGTREFCLK1P_226	SI5328_3_CLKIN2_P	MGT REFCLK	-
AJ10	MGTREFCLK0N_227	SI5328_3_CLKOUT1_PIN_N	MGT REFCLK	-
AJ11	MGTREFCLK0P_227	SI5328_3_CLKOUT1_PIN_P	MGT REFCLK	-
H39	MGTREFCLK0N_132	SI5328_3_CLKOUT2_PIN_N	MGT REFCLK	-
H38	MGTREFCLK0P_132	SI5328_3_CLKOUT2_PIN_P	MGT REFCLK	-
BA14	IO_L4P_AD8P_88	SI5328_3_INT_C1B	1.8	-
BB14	IO_L4N_AD8N_88	SI5328_3_LOL	1.8	-
AP14	IO_L11N_AD1N_88	SI5328_3_RST_L	1.8	-
AT13	IO_L9N_AD3N_88	SI5328_SCL	1.8	-
AT14	IO_L9P_AD3P_88	SI5328_SDA	1.8	-
L13	IO_L1P_AD15P_93	SPARE_SCL	1.8	-
K13	IO_L1N_AD15N_93	SPARE_SDA	1.8	-
M14	IO_L2P_AD14P_93	SPARE_WP	1.8	-
M16	IO_L4P_AD12P_93	SRVC_MD_L_1V8	1.8	-
H16	IO_L8N_HDGC_93	USR_SW_0	1.8	-
G16	IO_L9P_AD11P_93	USR_SW_1	1.8	-

Table 11 : AD01474 pinout

Appendix B: SFP delays

Trace Delay (ps)	Trace Length (mm)	FPGA Pin	FPGA Pin Name	Signal Name
414	71	AE45	MGTFRXP1_128	MGT_128_RX1_P
414	71	AE46	MGTFRXN1_128	MGT_128_RX1_N
435	74	AH44	MGTFRXN2_127	MGT_127_RX2_N
435	74	AH43	MGTFRXP2_127	MGT_127_RX2_P
443	76	AG45	MGTFRXP3_127	MGT_127_RX3_P
443	76	AG46	MGTFRXN3_127	MGT_127_RX3_N
444	76	AJ40	MGTFTXP3_127	MGT_127_TX3_P
444	76	AJ41	MGTFTXN3_127	MGT_127_TX3_N
448	77	AH38	MGTFTXP0_128	MGT_128_TX0_P
449	77	AH39	MGTFTXN0_128	MGT_128_TX0_N
453	77	AC45	MGTFRXP3_128	MGT_128_RX3_P
453	77	AC46	MGTFRXN3_128	MGT_128_RX3_N
458	78	AF43	MGTFRXP0_128	MGT_128_RX0_P
458	78	AF44	MGTFRXN0_128	MGT_128_RX0_N
481	82	AG40	MGTFTXP1_128	MGT_128_TX1_P
481	82	AK39	MGTFTXN2_127	MGT_127_TX2_N
481	82	AK38	MGTFTXP2_127	MGT_127_TX2_P
481	82	AG41	MGTFTXN1_128	MGT_128_TX1_N
495	85	AL40	MGTFTXP1_127	MGT_127_TX1_P
495	85	AL41	MGTFTXN1_127	MGT_127_TX1_N
499	85	AJ46	MGTFRXN1_127	MGT_127_RX1_N
499	85	AJ45	MGTFRXP1_127	MGT_127_RX1_P
500	85	AK44	MGTFRXN0_127	MGT_127_RX0_N
500	86	AK43	MGTFRXP0_127	MGT_127_RX0_P
520	89	AF38	MGTFTXP2_128	MGT_128_TX2_P
520	89	AF39	MGTFTXN2_128	MGT_128_TX2_N
522	89	AA45	MGTFRXP1_129	MGT_129_RX1_P
522	89	AA46	MGTFRXN1_129	MGT_129_RX1_N
531	91	AD43	MGTFRXP2_128	MGT_128_RX2_P
531	91	AD44	MGTFRXN2_128	MGT_128_RX2_N
539	92	AE40	MGTFTXP3_128	MGT_128_TX3_P
539	92	AE41	MGTFTXN3_128	MGT_128_TX3_N

Table 12 : SFP delays (continued on next page)

Trace Delay (ps)	Trace Length (mm)	FPGA Pin	FPGA Pin Name	Signal Name
548	94	AM38	MGTFTXP0_127	MGT_127_TX0_P
548	94	AM39	MGTFTXN0_127	MGT_127_TX0_N
572	98	AM44	MGTFRXN2_126	MGT_126_RX2_N
572	98	AM43	MGTFRXP2_126	MGT_126_RX2_P
573	98	AN41	MGTFTXN3_126	MGT_126_TX3_N
573	98	AN40	MGTFTXP3_126	MGT_126_TX3_P
575	98	AL46	MGTFRXN3_126	MGT_126_RX3_N
575	98	AL45	MGTFRXP3_126	MGT_126_RX3_P
591	101	AD38	MGTFTXP0_129	MGT_129_TX0_P
591	101	AD39	MGTFTXN0_129	MGT_129_TX0_N
594	101	W45	MGTFRXP3_129	MGT_129_RX3_P
597	102	W46	MGTFRXN3_129	MGT_129_RX3_N
603	103	AB43	MGTFRXP0_129	MGT_129_RX0_P
603	103	AB44	MGTFRXN0_129	MGT_129_RX0_N
606	103	AC40	MGTFTXP1_129	MGT_129_TX1_P
606	104	AC41	MGTFTXN1_129	MGT_129_TX1_N
620	106	AP38	MGTFTXP2_126	MGT_126_TX2_P
620	106	AP39	MGTFTXN2_126	MGT_126_TX2_N
639	109	AR41	MGTFTXN1_126	MGT_126_TX1_N
639	109	AR40	MGTFTXP1_126	MGT_126_TX1_P
643	110	AN46	MGTFRXN1_126	MGT_126_RX1_N
643	110	AN45	MGTFRXP1_126	MGT_126_RX1_P
644	110	AP43	MGTFRXP0_126	MGT_126_RX0_P
644	110	AP44	MGTFRXN0_126	MGT_126_RX0_N
663	113	AB38	MGTFTXP2_129	MGT_129_TX2_P
663	113	AB39	MGTFTXN2_129	MGT_129_TX2_N
667	114	U45	MGTFRXP1_130	MGT_130_RX1_P
667	114	U46	MGTFRXN1_130	MGT_130_RX1_N
675	115	Y43	MGTFRXP2_129	MGT_129_RX2_P
675	115	Y44	MGTFRXN2_129	MGT_129_RX2_N
678	116	AA40	MGTFTXP3_129	MGT_129_TX3_P
678	116	AA41	MGTFTXN3_129	MGT_129_TX3_N
692	118	AT38	MGTFTXP0_126	MGT_126_TX0_P
693	118	AT39	MGTFTXN0_126	MGT_126_TX0_N
715	122	AT44	MGTFRXN2_125	MGT_125_RX2_N

Table 12 : SFP delays (continued on next page)

Trace Delay (ps)	Trace Length (mm)	FPGA Pin	FPGA Pin Name	Signal Name
716	122	AT43	MGTFRXP2_125	MGT_125_RX2_P
716	122	AU40	MGTFTXP3_125	MGT_125_TX3_P
716	122	AU41	MGTFTXN3_125	MGT_125_TX3_N
720	123	AR45	MGTFRXP3_125	MGT_125_RX3_P
720	123	AR46	MGTFRXN3_125	MGT_125_RX3_N
735	126	Y39	MGTFTXN0_130	MGT_130_TX0_N
736	126	Y38	MGTFTXP0_130	MGT_130_TX0_P
741	127	R45	MGTFRXP3_130	MGT_130_RX3_P
741	127	R46	MGTFRXN3_130	MGT_130_RX3_N
750	128	V43	MGTFRXP0_130	MGT_130_RX0_P
750	128	V44	MGTFRXN0_130	MGT_130_RX0_N
750	128	W40	MGTFTXP1_130	MGT_130_TX1_P
751	128	W41	MGTFTXN1_130	MGT_130_TX1_N
756	129	AW41	MGTFTXN2_125	MGT_125_TX2_N
757	129	AW40	MGTFTXP2_125	MGT_125_TX2_P
787	134	AU45	MGTFRXP1_125	MGT_125_RX1_P
787	134	BA41	MGTFTXN1_125	MGT_125_TX1_N
787	134	AU46	MGTFRXN1_125	MGT_125_RX1_N
787	135	BA40	MGTFTXP1_125	MGT_125_TX1_P
787	135	AV44	MGTFRXN0_125	MGT_125_RX0_N
787	135	AV43	MGTFRXP0_125	MGT_125_RX0_P
807	138	V39	MGTFTXN2_130	MGT_130_TX2_N
809	138	V38	MGTFTXP2_130	MGT_130_TX2_P
809	138	N46	MGTFRXN1_131	MGT_131_RX1_N
809	138	N45	MGTFRXP1_131	MGT_131_RX1_P
820	140	BB42	MGTFTXP0_125	MGT_125_TX0_P
820	140	BB43	MGTFTXN0_125	MGT_125_TX0_N
822	140	T43	MGTFRXP2_130	MGT_130_RX2_P
822	140	T44	MGTFRXN2_130	MGT_130_RX2_N
822	141	U40	MGTFTXP3_130	MGT_130_TX3_P
823	141	U41	MGTFTXN3_130	MGT_130_TX3_N
854	146	BC40	MGTFTXP3_124	MGT_124_TX3_P
854	146	BC41	MGTFTXN3_124	MGT_124_TX3_N
859	147	AW46	MGTFRXN3_124	MGT_124_RX3_N
859	147	AW45	MGTFRXP3_124	MGT_124_RX3_P

Table 12 : SFP delays (continued on next page)

Trace Delay (ps)	Trace Length (mm)	FPGA Pin	FPGA Pin Name	Signal Name
861	147	AY44	MGTFRXN2_124	MGT_124_RX2_N
861	147	AY43	MGTFRXP2_124	MGT_124_RX2_P
877	150	T38	MGTFTXP0_131	MGT_131_TX0_P
877	150	L46	MGTFRXN3_131	MGT_131_RX3_N
877	150	T39	MGTFTXN0_131	MGT_131_TX0_N
877	150	L45	MGTFRXP3_131	MGT_131_RX3_P
889	152	R40	MGTFTXP1_131	MGT_131_TX1_P
889	152	R41	MGTFTXN1_131	MGT_131_TX1_N
892	152	P43	MGTFRXP0_131	MGT_131_RX0_P
892	152	P44	MGTFRXN0_131	MGT_131_RX0_N
894	153	BD43	MGTFTXN2_124	MGT_124_TX2_N
895	153	BD42	MGTFTXP2_124	MGT_124_TX2_P
915	156	BC45	MGTFRXP0_124	MGT_124_RX0_P
915	156	BC46	MGTFRXN0_124	MGT_124_RX0_N
928	159	BE40	MGTFTXP1_124	MGT_124_TX1_P
928	159	BE41	MGTFTXN1_124	MGT_124_TX1_N
930	159	BA45	MGTFRXP1_124	MGT_124_RX1_P
930	159	BA46	MGTFRXN1_124	MGT_124_RX1_N
948	162	P38	MGTFTXP2_131	MGT_131_TX2_P
948	162	P39	MGTFTXN2_131	MGT_131_TX2_N
961	164	BF43	MGTFTXN0_124	MGT_124_TX0_N
963	165	M44	MGTFRXN2_131	MGT_131_RX2_N
963	165	M43	MGTFRXP2_131	MGT_131_RX2_P
963	165	BF42	MGTFTXP0_124	MGT_124_TX0_P
966	165	N40	MGTFTXP3_131	MGT_131_TX3_P
966	165	N41	MGTFTXN3_131	MGT_131_TX3_N

Table 12 : SFP delays

Appendix C: QSFP delays

Delay (ps)	Length (mm)	FPGA Pin	FPGA Pin Name	Signal Name
1191	272	J2	MGTFRXP1_232	FIREFLY_1_RX1_P
1192	272	J1	MGTFRXN1_232	FIREFLY_1_RX1_N
1211	276	G1	MGTFRXN3_232	FIREFLY_1_RX3_N
1211	276	G2	MGTFRXP3_232	FIREFLY_1_RX3_P
1213	276	K3	MGTFRXN0_232	FIREFLY_1_RX0_N
1213	276	K4	MGTFRXP0_232	FIREFLY_1_RX0_P
1229	279	H3	MGTFRXN2_232	FIREFLY_1_RX2_N
1229	279	H4	MGTFRXP2_232	FIREFLY_1_RX2_P
1232	279	AA1	MGTFRXN1_229	FIREFLY_3_RX1_N
1232	279	AA2	MGTFRXP1_229	FIREFLY_3_RX1_P
1254	283	W1	MGTFRXN3_229	FIREFLY_3_RX3_N
1254	283	W2	MGTFRXP3_229	FIREFLY_3_RX3_P
1260	284	AB3	MGTFRXN0_229	FIREFLY_3_RX0_N
1260	284	AB4	MGTFRXP0_229	FIREFLY_3_RX0_P
1265	285	L6	MGTFTXN1_232	FIREFLY_1_TX1_N
1265	285	L7	MGTFTXP1_232	FIREFLY_1_TX1_P
1269	285	K8	MGTFTXN2_232	FIREFLY_1_TX2_N
1269	285	K9	MGTFTXP2_232	FIREFLY_1_TX2_P
1273	286	AB8	MGTFTXN2_229	FIREFLY_3_TX2_N
1273	286	AB9	MGTFTXP2_229	FIREFLY_3_TX2_P
1277	287	Y3	MGTFRXN2_229	FIREFLY_3_RX2_N
1277	287	Y4	MGTFRXP2_229	FIREFLY_3_RX2_P
1279	287	E1	MGTFRXN1_233	FIREFLY_0_RX1_N
1279	287	E2	MGTFRXP1_233	FIREFLY_0_RX1_P
1284	288	AA6	MGTFTXN3_229	FIREFLY_3_TX3_N
1284	288	AA7	MGTFTXP3_229	FIREFLY_3_TX3_P
1285	288	J6	MGTFTXN3_232	FIREFLY_1_TX3_N
1285	288	J7	MGTFTXP3_232	FIREFLY_1_TX3_P
1291	289	AC6	MGTFTXN1_229	FIREFLY_3_TX1_N
1292	289	AC7	MGTFTXP1_229	FIREFLY_3_TX1_P
1298	290	F3	MGTFRXN0_233	FIREFLY_0_RX0_N
1298	291	F4	MGTFRXP0_233	FIREFLY_0_RX0_P
1302	291	M9	MGTFTXP0_232	FIREFLY_1_TX0_P

Table 13 : QSFP delays (continued on next page)

Delay (ps)	Length (mm)	FPGA Pin	FPGA Pin Name	Signal Name
1303	291	M8	MGTFTXN0_232	FIREFLY_1_TX0_N
1307	292	B3	MGTFRXN3_233	FIREFLY_0_RX3_N
1307	292	B4	MGTFRXP3_233	FIREFLY_0_RX3_P
1321	294	D3	MGTFRXN2_233	FIREFLY_0_RX2_N
1321	294	D4	MGTFRXP2_233	FIREFLY_0_RX2_P
1335	297	AD8	MGTFTXN0_229	FIREFLY_3_TX0_N
1335	297	AD9	MGTFTXP0_229	FIREFLY_3_TX0_P
1337	297	C6	MGTFTXN2_233	FIREFLY_0_TX2_N
1337	297	C7	MGTFTXP2_233	FIREFLY_0_TX2_P
1357	301	A6	MGTFTXN3_233	FIREFLY_0_TX3_N
1357	301	A7	MGTFTXP3_233	FIREFLY_0_TX3_P
1361	301	N1	MGTFRXN1_231	FIREFLY_2_RX1_N
1361	301	N2	MGTFRXP1_231	FIREFLY_2_RX1_P
1371	303	E6	MGTFTXN1_233	FIREFLY_0_TX1_N
1371	303	E7	MGTFTXP1_233	FIREFLY_0_TX1_P
1386	305	P3	MGTFRXN0_231	FIREFLY_2_RX0_N
1386	305	P4	MGTFRXP0_231	FIREFLY_2_RX0_P
1390	306	L1	MGTFRXN3_231	FIREFLY_2_RX3_N
1390	306	L2	MGTFRXP3_231	FIREFLY_2_RX3_P
1393	307	AE1	MGTFRXN1_228	FIREFLY_5_RX1_N
1393	307	AE2	MGTFRXP1_228	FIREFLY_5_RX1_P
1395	307	P8	MGTFTXN2_231	FIREFLY_2_TX2_N
1395	307	P9	MGTFTXP2_231	FIREFLY_2_TX2_P
1405	309	R6	MGTFTXN1_231	FIREFLY_2_TX1_N
1405	309	R7	MGTFTXP1_231	FIREFLY_2_TX1_P
1408	309	M4	MGTFRXP2_231	FIREFLY_2_RX2_P
1409	309	M3	MGTFRXN2_231	FIREFLY_2_RX2_N
1411	310	G6	MGTFTXN0_233	FIREFLY_0_TX0_N
1411	310	G7	MGTFTXP0_233	FIREFLY_0_TX0_P
1411	310	N6	MGTFTXN3_231	FIREFLY_2_TX3_N
1411	310	N7	MGTFTXP3_231	FIREFLY_2_TX3_P
1412	310	AF8	MGTFTXN2_228	FIREFLY_5_TX2_N
1413	310	AF9	MGTFTXP2_228	FIREFLY_5_TX2_P
1413	310	AE6	MGTFTXN3_228	FIREFLY_5_TX3_N
1413	310	AE7	MGTFTXP3_228	FIREFLY_5_TX3_P
1417	311	AF3	MGTFRXN0_228	FIREFLY_5_RX0_N

Table 13 : QSFP delays (continued on next page)

Delay (ps)	Length (mm)	FPGA Pin	FPGA Pin Name	Signal Name
1417	311	AF4	MGTFRXP0_228	FIREFLY_5_RX0_P
1418	311	AC2	MGTFRXP3_228	FIREFLY_5_RX3_P
1419	311	AC1	MGTFRXN3_228	FIREFLY_5_RX3_N
1438	314	AG6	MGTFTXN1_228	FIREFLY_5_TX1_N
1438	314	AG7	MGTFTXP1_228	FIREFLY_5_TX1_P
1445	315	AD3	MGTFRXN2_228	FIREFLY_5_RX2_N
1445	315	AD4	MGTFRXP2_228	FIREFLY_5_RX2_P
1447	316	T8	MGTFTXN0_231	FIREFLY_2_TX0_N
1447	316	T9	MGTFTXP0_231	FIREFLY_2_TX0_P
1452	317	AT8	MGTFTXN0_226	FIREFLY_7_TX0_N
1452	317	AT9	MGTFTXP0_226	FIREFLY_7_TX0_P
1469	320	AP8	MGTFTXN2_226	FIREFLY_7_TX2_N
1470	320	AP9	MGTFTXP2_226	FIREFLY_7_TX2_P
1474	320	U1	MGTFRXN1_230	FIREFLY_4_RX1_N
1474	320	U2	MGTFRXP1_230	FIREFLY_4_RX1_P
1479	321	AH8	MGTFTXN0_228	FIREFLY_5_TX0_N
1479	321	AH9	MGTFTXP0_228	FIREFLY_5_TX0_P
1491	323	AR6	MGTFTXN1_226	FIREFLY_7_TX1_N
1491	323	AR7	MGTFTXP1_226	FIREFLY_7_TX1_P
1498	325	V3	MGTFRXN0_230	FIREFLY_4_RX0_N
1498	325	V4	MGTFRXP0_230	FIREFLY_4_RX0_P
1504	326	R1	MGTFRXN3_230	FIREFLY_4_RX3_N
1504	325	R2	MGTFRXP3_230	FIREFLY_4_RX3_P
1505	326	V8	MGTFTXN2_230	FIREFLY_4_TX2_N
1505	326	V9	MGTFTXP2_230	FIREFLY_4_TX2_P
1509	326	AN6	MGTFTXN3_226	FIREFLY_7_TX3_N
1509	326	AN7	MGTFTXP3_226	FIREFLY_7_TX3_P
1519	328	T3	MGTFRXN2_230	FIREFLY_4_RX2_N
1519	328	T4	MGTFRXP2_230	FIREFLY_4_RX2_P
1521	329	U6	MGTFTXN3_230	FIREFLY_4_TX3_N
1521	329	U7	MGTFTXP3_230	FIREFLY_4_TX3_P
1525	329	W6	MGTFTXN1_230	FIREFLY_4_TX1_N
1525	329	W7	MGTFTXP1_230	FIREFLY_4_TX1_P
1528	330	AM8	MGTFTXN0_227	FIREFLY_6_TX0_N
1528	330	AM9	MGTFTXP0_227	FIREFLY_6_TX0_P
1545	333	AK8	MGTFTXN2_227	FIREFLY_6_TX2_N

Table 13 : QSFP delays **(continued on next page)**

Delay (ps)	Length (mm)	FPGA Pin	FPGA Pin Name	Signal Name
1545	333	AK9	MGTFTXP2_227	FIREFLY_6_TX2_P
1566	336	AL6	MGTFTXN1_227	FIREFLY_6_TX1_N
1566	336	AL7	MGTFTXP1_227	FIREFLY_6_TX1_P
1567	336	AL1	MGTFRXN3_226	FIREFLY_7_RX3_N
1567	336	AL2	MGTFRXP3_226	FIREFLY_7_RX3_P
1569	337	AM3	MGTFRXN2_226	FIREFLY_7_RX2_N
1569	337	AM4	MGTFRXP2_226	FIREFLY_7_RX2_P
1570	337	Y9	MGTFTXP0_230	FIREFLY_4_TX0_P
1570	337	Y8	MGTFTXN0_230	FIREFLY_4_TX0_N
1581	339	AP3	MGTFRXN0_226	FIREFLY_7_RX0_N
1581	339	AP4	MGTFRXP0_226	FIREFLY_7_RX0_P
1590	340	AJ6	MGTFTXN3_227	FIREFLY_6_TX3_N
1590	340	AJ7	MGTFTXP3_227	FIREFLY_6_TX3_P
1618	345	AN1	MGTFRXN1_226	FIREFLY_7_RX1_N
1618	345	AN2	MGTFRXP1_226	FIREFLY_7_RX1_P
1644	349	AK3	MGTFRXN0_227	FIREFLY_6_RX0_N
1644	349	AK4	MGTFRXP0_227	FIREFLY_6_RX0_P
1644	350	AH3	MGTFRXN2_227	FIREFLY_6_RX2_N
1644	350	AH4	MGTFRXP2_227	FIREFLY_6_RX2_P
1652	351	AG1	MGTFRXN3_227	FIREFLY_6_RX3_N
1652	351	AG2	MGTFRXP3_227	FIREFLY_6_RX3_P
1685	357	AJ1	MGTFRXN1_227	FIREFLY_6_RX1_N
1685	357	AJ2	MGTFRXP1_227	FIREFLY_6_RX1_P
2013	426	G46	MGTFRXN3_132	FIREFLY_8_RX3_N
2013	426	G45	MGTFRXP3_132	FIREFLY_8_RX3_P
2020	428	H44	MGTFRXN2_132	FIREFLY_8_RX2_N
2020	428	H43	MGTFRXP2_132	FIREFLY_8_RX2_P
2023	428	A41	MGTFTXN3_133	FIREFLY_9_TX3_N
2023	428	A40	MGTFTXP3_133	FIREFLY_9_TX3_P
2026	429	D44	MGTFRXN2_133	FIREFLY_9_RX2_N
2026	429	D43	MGTFRXP2_133	FIREFLY_9_RX2_P
2031	429	K44	MGTFRXN0_132	FIREFLY_8_RX0_N
2031	429	K43	MGTFRXP0_132	FIREFLY_8_RX0_P
2031	429	B44	MGTFRXN3_133	FIREFLY_9_RX3_N
2031	429	B43	MGTFRXP3_133	FIREFLY_9_RX3_P
2035	430	F44	MGTFRXN0_133	FIREFLY_9_RX0_N

Table 13 : QSFP delays **(continued on next page)**

Delay (ps)	Length (mm)	FPGA Pin	FPGA Pin Name	Signal Name
2035	430	F43	MGTFRXP0_133	FIREFLY_9_RX0_P
2045	432	E46	MGTFRXN1_133	FIREFLY_9_RX1_N
2045	432	E45	MGTFRXP1_133	FIREFLY_9_RX1_P
2047	432	C41	MGTFTXN2_133	FIREFLY_9_TX2_N
2047	432	C40	MGTFTXP2_133	FIREFLY_9_TX2_P
2049	433	E41	MGTFTXN1_133	FIREFLY_9_TX1_N
2049	433	E40	MGTFTXP1_133	FIREFLY_9_TX1_P
2074	437	J45	MGTFRXP1_132	FIREFLY_8_RX1_P
2075	437	J46	MGTFRXN1_132	FIREFLY_8_RX1_N
2081	438	J41	MGTFTXN3_132	FIREFLY_8_TX3_N
2081	438	J40	MGTFTXP3_132	FIREFLY_8_TX3_P
2086	439	G41	MGTFTXN0_133	FIREFLY_9_TX0_N
2086	439	G40	MGTFTXP0_133	FIREFLY_9_TX0_P
2117	444	K39	MGTFTXN2_132	FIREFLY_8_TX2_N
2117	444	K38	MGTFTXP2_132	FIREFLY_8_TX2_P
2144	449	M39	MGTFTXN0_132	FIREFLY_8_TX0_N
2144	449	M38	MGTFTXP0_132	FIREFLY_8_TX0_P
2187	456	L40	MGTFTXP1_132	FIREFLY_8_TX1_P
2188	456	L41	MGTFTXN1_132	FIREFLY_8_TX1_N

Table 13 : QSFP delays

Appendix D: System Sensors and Monitoring

		Access Standby			Full Power		
Device	Sensor	BMCEth	Front Panel USB	Front Panel UART	CPUEth	CPUApp	FPGA
ROMED4D-2T (MB)	3VSB	Y	TBD	Y	BMC	BMC	N
	5VSB	Y	TBD	Y	BMC	BMC	N
	VCPU	Y	TBD	Y	BMC	BMC	N
	VSOC	Y	TBD	Y	BMC	BMC	N
	VCCM ABCD	Y	TBD	Y	BMC	BMC	N
	VCCM EFGH	Y	TBD	Y	BMC	BMC	N
	VPPM ABCD	Y	TBD	Y	BMC	BMC	N
	VPPM EFGH	Y	TBD	Y	BMC	BMC	N
	LAN_1.2V	Y	TBD	Y	BMC	BMC	N
	1.8VSB	Y	TBD	Y	BMC	BMC	N
	1.8V	Y	TBD	Y	BMC	BMC	N
	BAT	Y	TBD	Y	BMC	BMC	N
	3V	Y	TBD	Y	BMC	BMC	N
	5V	Y	TBD	Y	BMC	BMC	N
	12V	Y	TBD	Y	BMC	BMC	N
	LAN_0.83V	Y	TBD	Y	BMC	BMC	N
MB-PSU(PMBus)	PSU1 VIN	Y	TBD	Y	BMC	BMC	N
	PSU2 VIN	Y	TBD	Y	BMC	BMC	N
	PSU1 IOUT	Y	TBD	Y	BMC	BMC	N
	PSU2 IOUT	Y	TBD	Y	BMC	BMC	N
IPMI	CPU1 Temp	Y	TBD	Y	BMC	BMC	N
	MB Temp	Y	TBD	Y	BMC	BMC	N
	Card Side Temp	Y	TBD	Y	BMC	BMC	N
	DDR4_A Temp	Y	TBD	Y	BMC	BMC	N
	DDR4_B Temp	Y	TBD	Y	BMC	BMC	N
	CPU1_PROCHOT	Y	TBD	Y	BMC	BMC	N
	CPU1_THERMTRIP	Y	TBD	Y	BMC	BMC	N
	CPU2_PROCHOT	Y	TBD	Y	BMC	BMC	N
	CPU2_THERMTRIP	Y	TBD	Y	BMC	BMC	N
	CPU_CATERR	Y	TBD	Y	BMC	BMC	N
	Chassisintr	Y	TBD	Y	BMC	BMC	N
	PSU1 ACLost	Y	TBD	Y	BMC	BMC	N
	PSU1 Status	Y	TBD	Y	BMC	BMC	N
	PSU2 ACLost	Y	TBD	Y	BMC	BMC	N
	PSU2 Status	Y	TBD	Y	BMC	BMC	N
	FAN related sensors(...)	Y	TBD	Y	BMC	BMC	N

Device	Sensor						
RPSU + PDB (PMBus)	CAPABILITY	Y	TBD	Y	BMC	BMC	N
	VOUT_MODE	Y	TBD	Y	BMC	BMC	N
	STATUS_WORD	Y	TBD	Y	BMC	BMC	N
	STATUS_12V_VOUT	Y	TBD	Y	BMC	BMC	N
	STATUS_12V_IOUT	Y	TBD	Y	BMC	BMC	N
	STATUS_TEMPERATURE	Y	TBD	Y	BMC	BMC	N
	STATUS_MFR_SPECIFIC	Y	TBD	Y	BMC	BMC	N
	READ_12V_VOUT	Y	TBD	Y	BMC	BMC	N
	READ_12V_IOUT	Y	TBD	Y	BMC	BMC	N
	READ_TEMPERATURE_1(1)	Y	TBD	Y	BMC	BMC	N
	READ_12V_POUT	Y	TBD	Y	BMC	BMC	N
	MFR_ID	Y	TBD	Y	BMC	BMC	N
	MFR_MODEL	Y	TBD	Y	BMC	BMC	N
	MFR_REVSION	Y	TBD	Y	BMC	BMC	N
	MFR_SERIAL	Y	TBD	Y	BMC	BMC	N
	MFR_POUT_MAX	Y	TBD	Y	BMC	BMC	N
	MFR_AMBIENT_MAX	Y	TBD	Y	BMC	BMC	N
	STATUS_PDB	Y	TBD	Y	BMC	BMC	N
	READ_3V3_VOUT	Y	TBD	Y	BMC	BMC	N
	READ_3V3_IOUT	Y	TBD	Y	BMC	BMC	N
	READ_3V3_POUT	Y	TBD	Y	BMC	BMC	N
	READ_5V_VOUT	Y	TBD	Y	BMC	BMC	N
	READ_5V_IOUT	Y	TBD	Y	BMC	BMC	N
	READ_5V_POUT	Y	TBD	Y	BMC	BMC	N
	VOUT_OV_FAULT(12V)	Y	TBD	Y	BMC	BMC	N
	VOUT_OV_WARNING(12V)	Y	TBD	Y	BMC	BMC	N
	VOUT_UV_WARNING(12V)	Y	TBD	Y	BMC	BMC	N
	VOUT_UV_FAULT(12V)	Y	TBD	Y	BMC	BMC	N
	IOUT_OC_FAULT(12V)	Y	TBD	Y	BMC	BMC	N
	IOUT_OC_WARNING(12V)	Y	TBD	Y	BMC	BMC	N
	3V3_UV_FAULT	Y	TBD	Y	BMC	BMC	N
	3V3_OV_FAULT	Y	TBD	Y	BMC	BMC	N
	5V_UV_FAULT	Y	TBD	Y	BMC	BMC	N
	5V_OV_FAULT	Y	TBD	Y	BMC	BMC	N
	3V3_IOUT_OC_ FAULT	Y	TBD	Y	BMC	BMC	N
	3V3_IOUT_OC_ WARNING	Y	TBD	Y	BMC	BMC	N
	5V_IOUT_OC_ FAULT	Y	TBD	Y	BMC	BMC	N
	5V_IOUT_OC_ WARNING	Y	TBD	Y	BMC	BMC	N
	PSU1_FAULT	Y	TBD	Y	BMC	BMC	N
	PSU2_FAULT	Y	TBD	Y	BMC	BMC	N
	PSU1 PLUG-IN/OUT_STATUS	Y	TBD	Y	BMC	BMC	N
	PSU2 PLUG-IN/OUT _STATUS	Y	TBD	Y	BMC	BMC	N
	POWER_GOOD#	Y	TBD	Y	BMC	BMC	N
	PSON#	Y	TBD	Y	BMC	BMC	N
	MFR_ID	Y	TBD	Y	BMC	BMC	N
	MFR_MODEL	Y	TBD	Y	BMC	BMC	N
	MFR_REVSION	Y	TBD	Y	BMC	BMC	N
	MFR_SERIAL	Y	TBD	Y	BMC	BMC	N

	MFR_POUT_MAX	Y	TBD	Y	BMC	BMC	N
	MFR_AMBIENT_MAX	Y	TBD	Y	BMC	BMC	N
	PSUPDB Device	Y	TBD	Y	BMC	BMC	N
Device	Sensor						
	ETC	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	EC	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC00(12V AUXrail)	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC01(12V rail)	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC02(12V current)	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC03(3.3V AUXrail)	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC04(3.3V rail)	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC05(3.3V VCCOrail (internal))	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC06(1.8V rail (internal))	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC07(1.5V rail (internal))	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC08(1.5V AUXrail (internal))	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC09(1.2V AVTT (internal))	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC10(1.2V rail (internal))	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC11 (0.88V AVCC(internal))	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC12(FPGAcore rail (internal))	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC13(FMCVAdj rail (internal))	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	TMP00 (uCinternal temp.(°C))	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	TMP01 (Board temp.(°C))	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	TMP02 (Board temp.(°C))	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	TMP03 (FPGAtemp.(°C))	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	MEZ_STAT0	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	MEZ_STAT1	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	MEZ_STAT2	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
AD01474	MEZ_STAT3	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
(FPGA)	CRD_STAT0	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	CRD_STAT1	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	CRD_STAT2	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	CRD_STAT3	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	SI5338_STAT	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	SI5338_ERR	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC_STAT00	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC_STAT01	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC_STAT02	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC_STAT03	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC_STAT04	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC_STAT05	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC_STAT06	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC_STAT07	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC_STAT08	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC_STAT09	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC_STAT10	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC_STAT11	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC_STAT12	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	ADC_STAT13	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	TMP_STAT00	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	TMP_STAT01	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	TMP_STAT02	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
	TMP_STAT03	IPMI	Y	N	IPMI/USB	IPMI/USB	AVR
AD01475	tx_fault	N	N	N	IPMI/USB	IPMI/USB	Y
32x SFP	tx_disable	N	N	N	IPMI/USB	IPMI/USB	Y
	mod_abs	IPMI	Y	IPMI	IPMI/USB	IPMI/USB	Y
	rs0	N	N	N	IPMI/USB	IPMI/USB	Y
	rx_los	N	N	N	IPMI/USB	IPMI/USB	Y
	rs1	N	N	N	IPMI/USB	IPMI/USB	Y
	Module I2C	N	N	N	IPMI/USB	IPMI/USB	Y
	Link Active LED	N	N	N	IPMI/USB	IPMI/USB	Y-R/W
AD01476	ModSelL	N	N	N	IPMI/USB	IPMI/USB	Y
2xQSFPx5	ResetL	N	N	N	IPMI/USB	IPMI/USB	Y
	ModPrsL	IPMI	Y	IPMI	IPMI/USB	IPMI/USB	Y
	IntL	N	N	N	IPMI/USB	IPMI/USB	Y
	LPMode	N	N	N	IPMI/USB	IPMI/USB	Y
	Module I2C	N	N	N	IPMI/USB	IPMI/USB	Y
	Link Active LED	N	N	N	IPMI/USB	IPMI/USB	Y- R/W

Key:

Y	Can access directly	AVR	FPGA accesses AVR UART interface
N	Access not possible	Y- R/W	FPGA sets the LED/Status
IPMI	BMC accesses via AVR IPMI	TBD	May be supported if USB UART access from FPGA USB to CPU UART in
USB	CPU access via AVR USB		
BMC	CPU accesses BMC		
IPMI/USB	CPU access via AVR USB or BMC IPMI		

Figure 26 : Sensors list with access options based on power profiles

Revision History

Date	Revision	Changed By	Nature of Change
23/05/23	1.0	C. Gutierrez - K. Roth	Issued
05/07/23	1.1	C. Gutierrez - K. Roth	Added complete FPGA pinout and QSFP/SFP cages connection to the FPGA (QUADs)
10/10/23	1.2	K. Roth	Updated language in Product Description, corrected line rate speeds throughout (25Gbps max for SFP/QSFP), deleted reduntant note about USB muxing at front panel, added size weight and power to Product Description, Expanded Feature Description to include Clocking, DDR4 SDRAM SODIMM, QDRII+,1PPS circuit, and delays for QSFP/SFP.

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